

COMPAL CONFIDENTIAL

MODEL NAME : *QCZ00* *Vinafix.com*
PCB NO : *LA-8831P*
BOM P/N : *TBD*
GPIO MAP:

Fei Dao 14 UMA

Ivy Bridge + Panther POINT

2012-09-13
REV : 1.0(A00)
@ : Nopop Component
CONN@ : Connector Component


MB Type	BOM P/N	
M/B SPI ROM		5@
TAA SPI ROM		6@
TPM ROM		TPM@
DTP ROM		DTP@
w/ eSATA Redriver		7@
w/o eSATA Redriver		8@
MB SPI ROM part		X76@
XDP(ITP) select		XDP@

MB Type	BOM config
w/ TPM + w/o TAA	TPM@+5@+X76@
w/o TPM + w/o TAA	DTP@+5@+X76@
w/ TPM + w/ TAA	TPM@+6@
w/o TPM + w/ TAA	DTP@+6@

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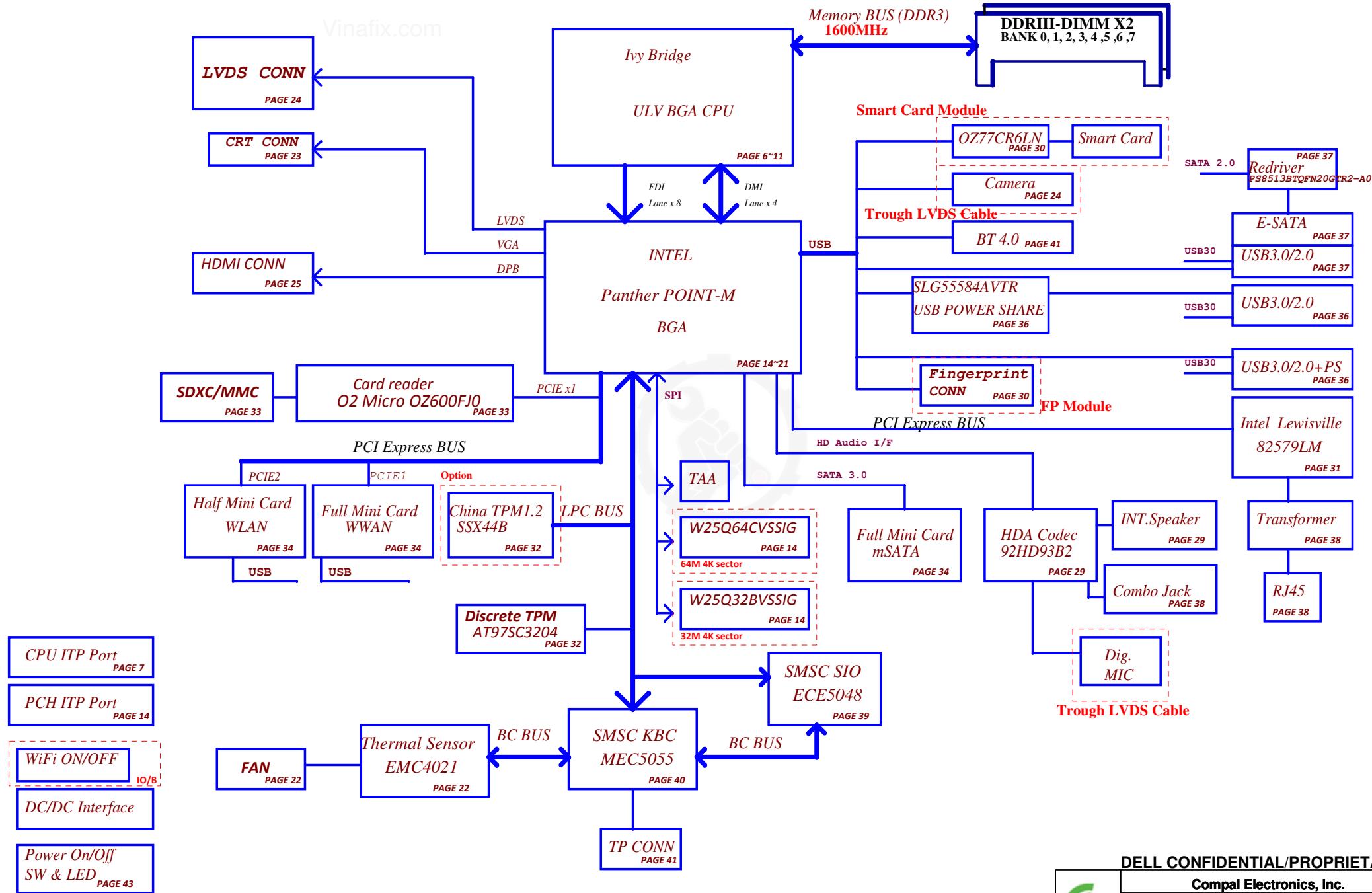
@HDMI Royalty	
Part Number	Description
RO0000002HM	HDMI Royalty

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Block Diagram



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UMA Block Diagram			
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB 3.0 PORT#	Connetion
1	JUSB1 (Right side)
2	JUSB3 (Left side)
3	JESA1 (Back side)
4	NA

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side)
	1	JUSB3 (Bot side)
	2	Top side E-SATA (Back side)
	3	
	4	WLAN
	5	WWAN
	6	
	7	Smart Card
	8	
	9	
	10	
	11	Blue Tooth
	12	Camera
	13	Finger Print

PM TABLE

power plane State	+PWR_SRC_S +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF


need to update Power Status
and PM Table

SATA	DESTINATION
SATA 0	mSATA
SATA 1	NA
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	NA

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	None
Lane 4	None
Lane 5	MINI CARD-3 mSATA
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	NA
Port D	NA

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Index and Config.

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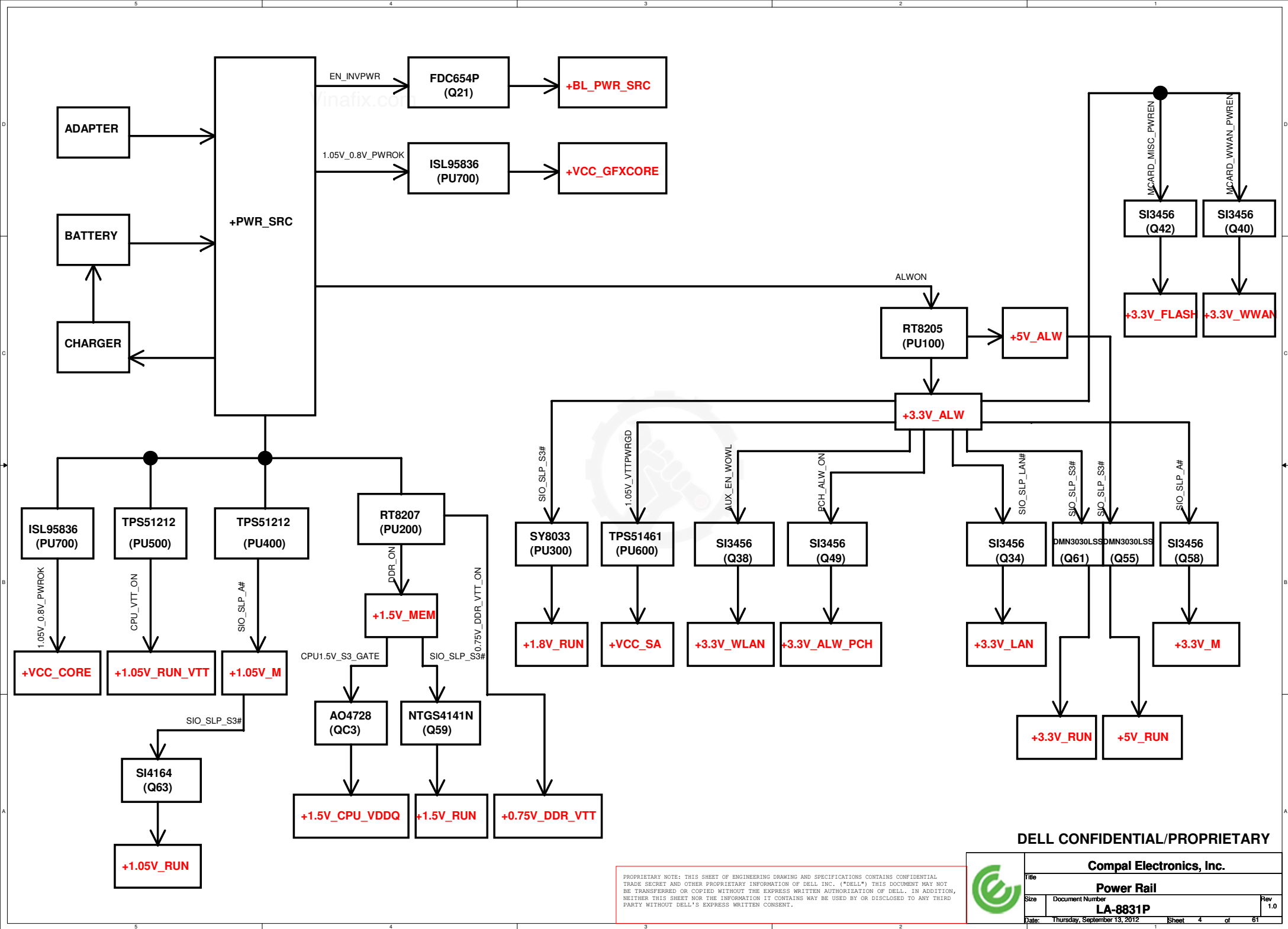
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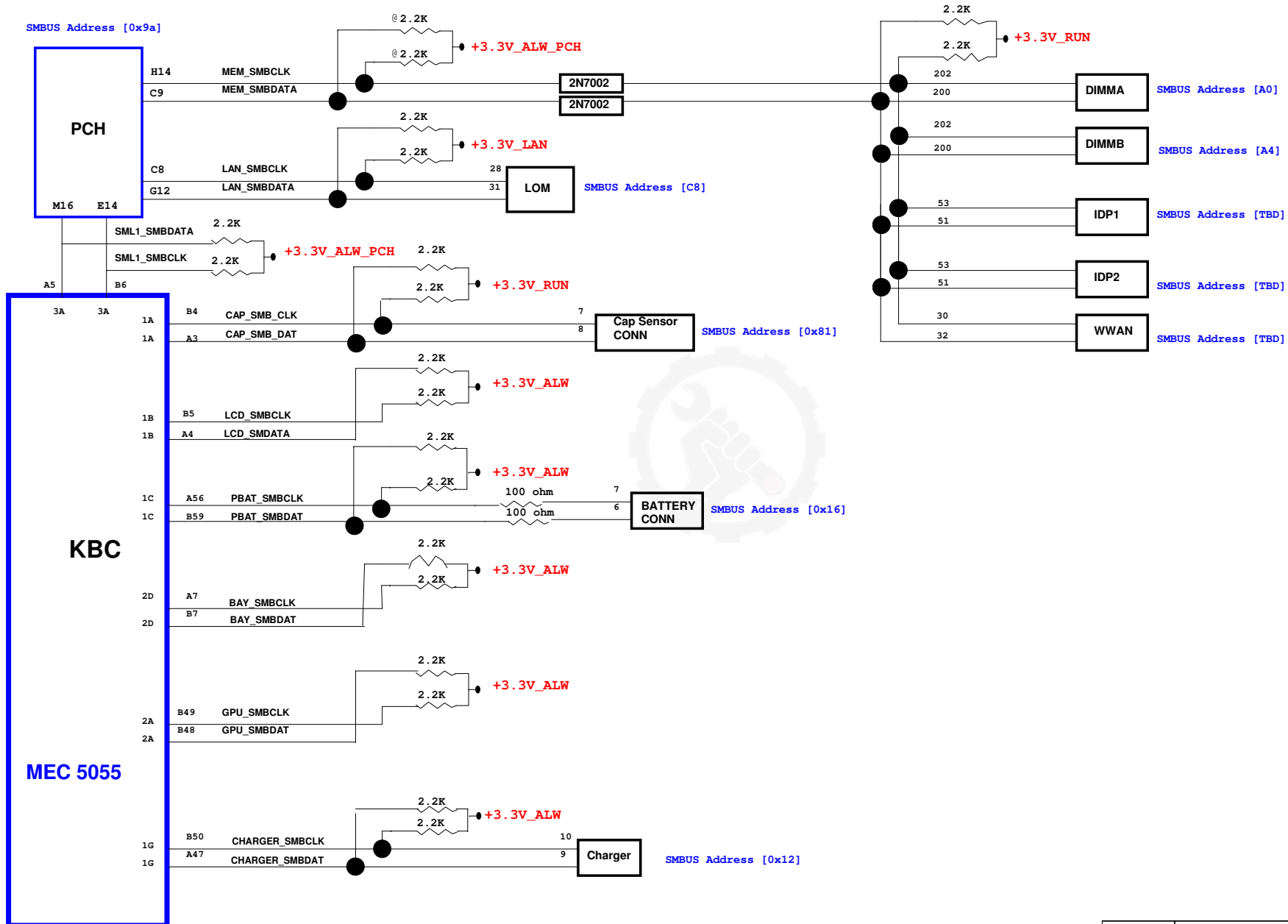
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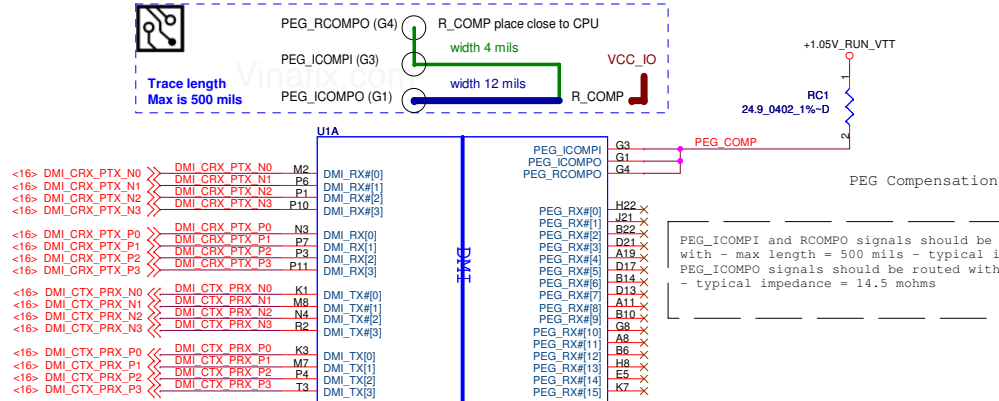
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- (1) PEG_RCOMP (G4) use 4mil connect to PEG_ICOMPI, then use 4mil connect to RC1.
(2) PEG_ICOMPO use 12mil connect to RC1



<16> DMI_CRX_PTX_N0 DMI_CRX_PTX_N0 M2 DMI_RX#0
<16> DMI_CRX_PTX_N1 DMI_CRX_PTX_N1 P6 DMI_RX#1
<16> DMI_CRX_PTX_N2 DMI_CRX_PTX_N2 P7 DMI_RX#2
<16> DMI_CRX_PTX_N3 DMI_CRX_PTX_N3 P10 DMI_RX#3

<16> DMI_CRX_PTX_P0 DMI_CRX_PTX_P1 N3 DMI_RX0
<16> DMI_CRX_PTX_P1 DMI_CRX_PTX_P2 P2 DMI_RX1
<16> DMI_CRX_PTX_P2 DMI_CRX_PTX_P3 P11 DMI_RX2
<16> DMI_CRX_PTX_P3 DMI_CRX_PTX_P3 P11 DMI_RX3

<16> DMI_CTX_PRX_N0 K1 DMI_TX#0
<16> DMI_CTX_PRX_N1 M8 DMI_TX#1
<16> DMI_CTX_PRX_N2 N4 DMI_TX#2
<16> DMI_CTX_PRX_N3 R2 DMI_TX#3

<16> DMI_CTX_PRX_P0 K3 DMI_TX0
<16> DMI_CTX_PRX_P1 M7 DMI_TX1
<16> DMI_CTX_PRX_P2 P4 DMI_TX2
<16> DMI_CTX_PRX_P3 T3 DMI_TX3

<16> FDI_CTX_PRX_N0 FDI_CTX_PRX_N0 U7 FDI0_TX#0
<16> FDI_CTX_PRX_N1 W11 FDI0_TX#1
<16> FDI_CTX_PRX_N2 W1 FDI0_TX#2
<16> FDI_CTX_PRX_N3 AA6 FDI0_TX#3
<16> FDI_CTX_PRX_N4 W6 FDI0_TX#4
<16> FDI_CTX_PRX_N5 V4 FDI0_TX#5
<16> FDI_CTX_PRX_N6 Y2 FDI0_TX#6
<16> FDI_CTX_PRX_N7 AC9 FDI0_TX#7

<16> FDI_CTX_PRX_P0 U8 FDI0_TX#0
<16> FDI_CTX_PRX_P1 W10 FDI0_TX#1
<16> FDI_CTX_PRX_P2 W3 FDI0_TX#2
<16> FDI_CTX_PRX_P3 AA7 FDI0_TX#3
<16> FDI_CTX_PRX_P4 W7 FDI0_TX#4
<16> FDI_CTX_PRX_P5 T4 FDI0_TX#5
<16> FDI_CTX_PRX_P6 AA3 FDI0_TX#6
<16> FDI_CTX_PRX_P7 AC9 FDI0_TX#7

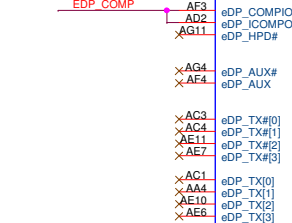
<16> FDI_FSYNCO FDI_FSYNCO AA11 FDI0_FSYNC
<16> FDI_FSYNC1 FDI_FSYNC1 AC12 FDI0_FSYNC

<16> FDI_INT FDI_INT U11 FDI_INT

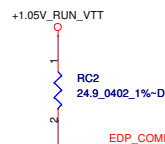
<16> FDI_LSYNCO FDI_LSYNCO AA10 FDI0_LSYNC
<16> FDI_LSYNC1 FDI_LSYNC1 AG8 FDI0_LSYNC

(1) EDP_COMPIO use 4mil trace to RC1

(2) EDP_ICOMPO use 12mil trace to RC1



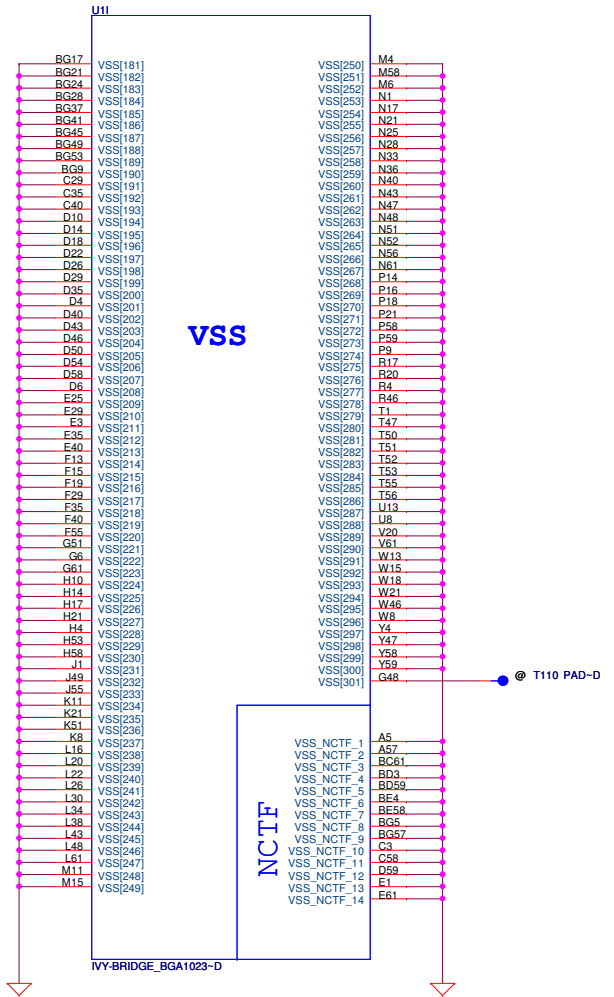
eDP Compensation



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PCI EXPRESS -- GRAPHICS

IVY-BRIDGE_BGA1023-D



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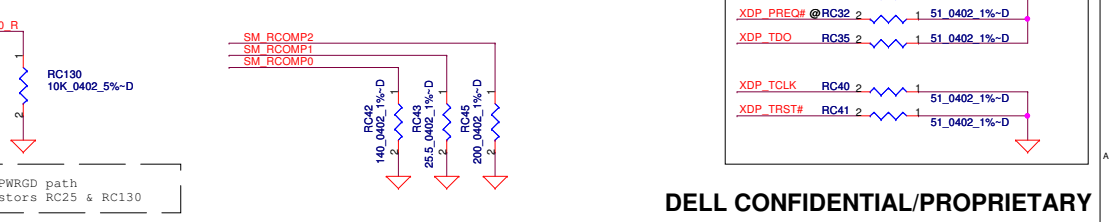
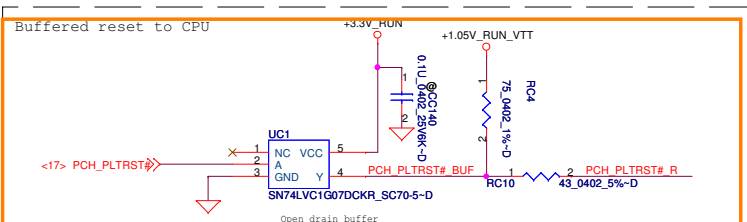
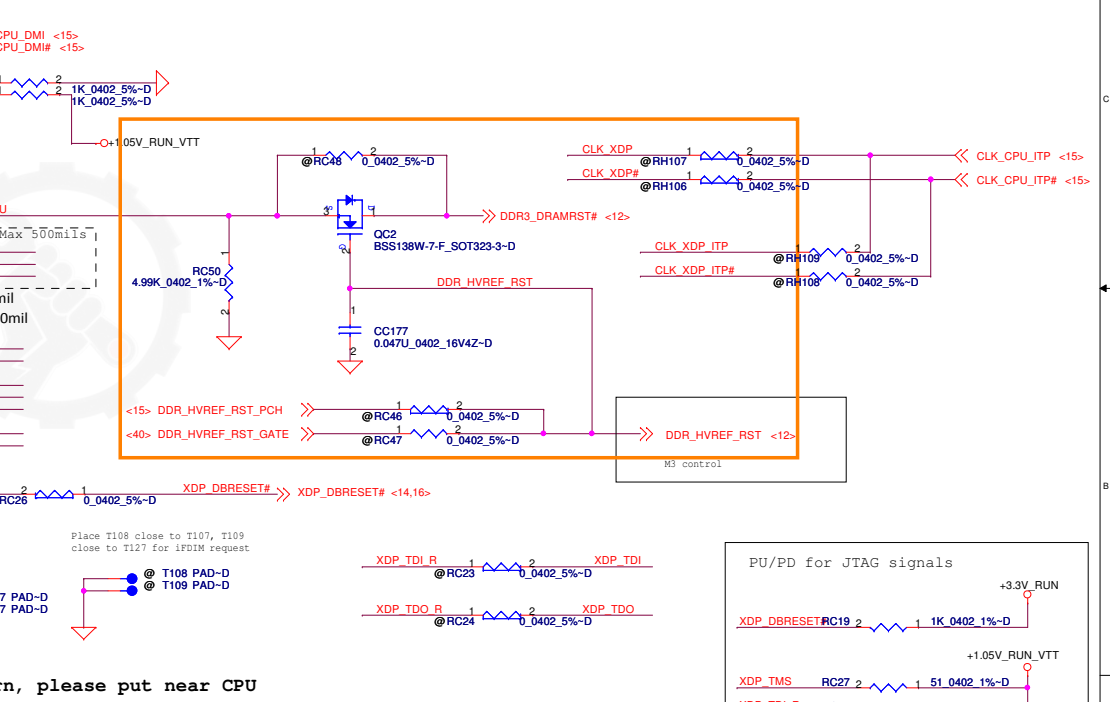
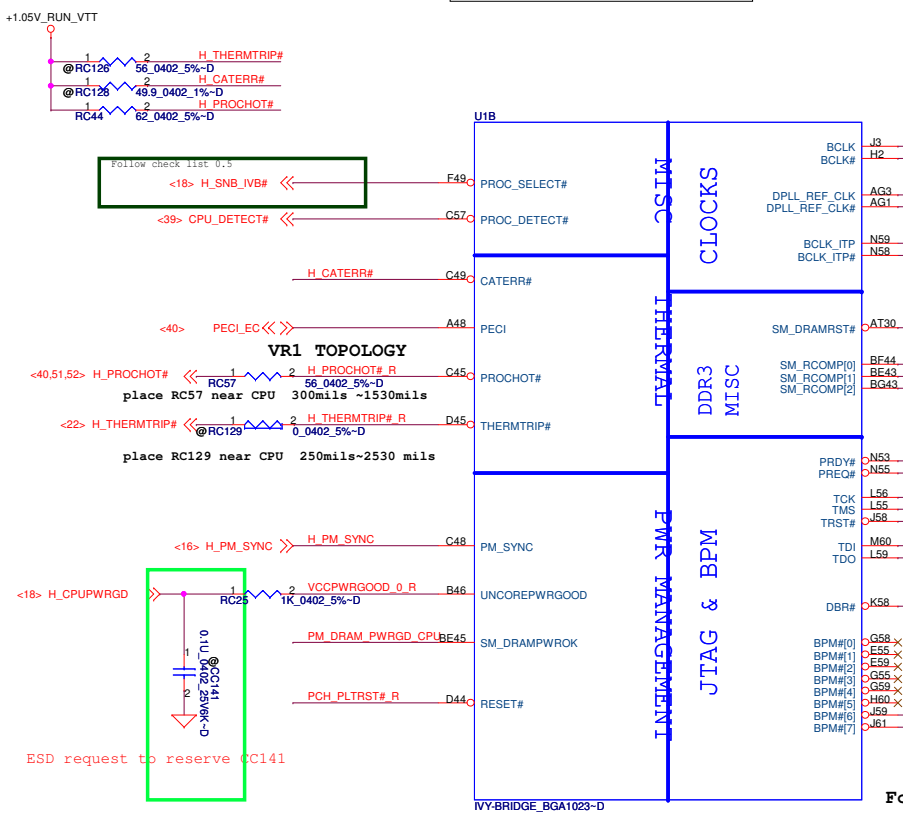
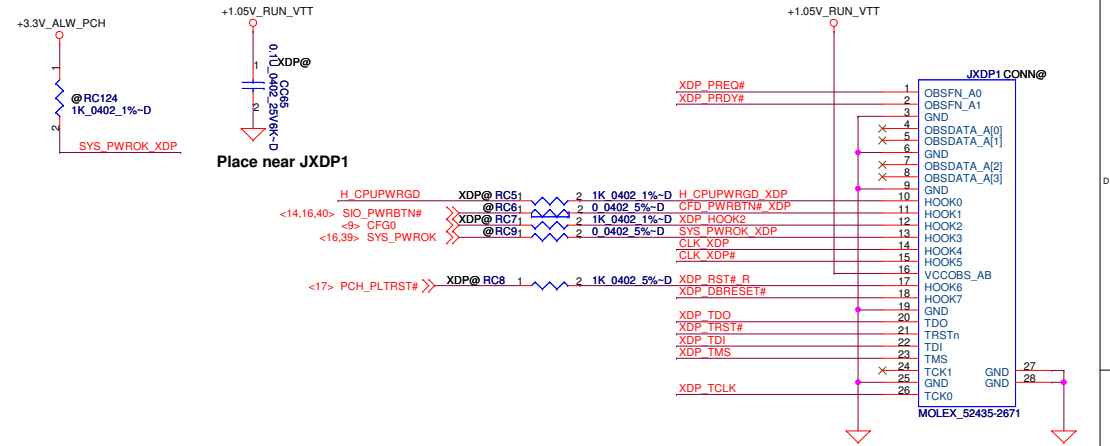
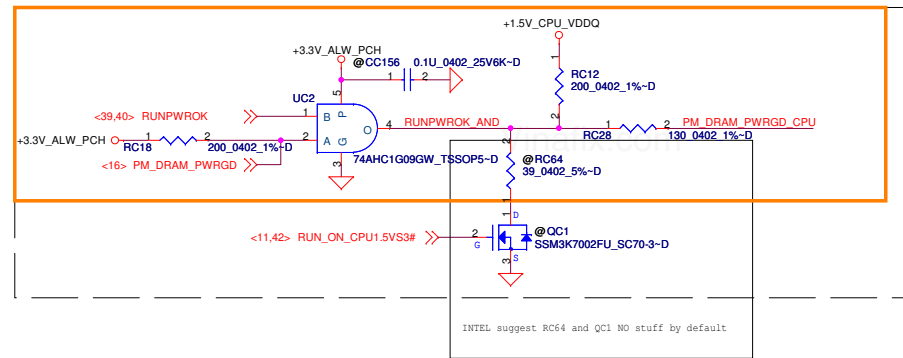
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Ivy Bridge (1/6)

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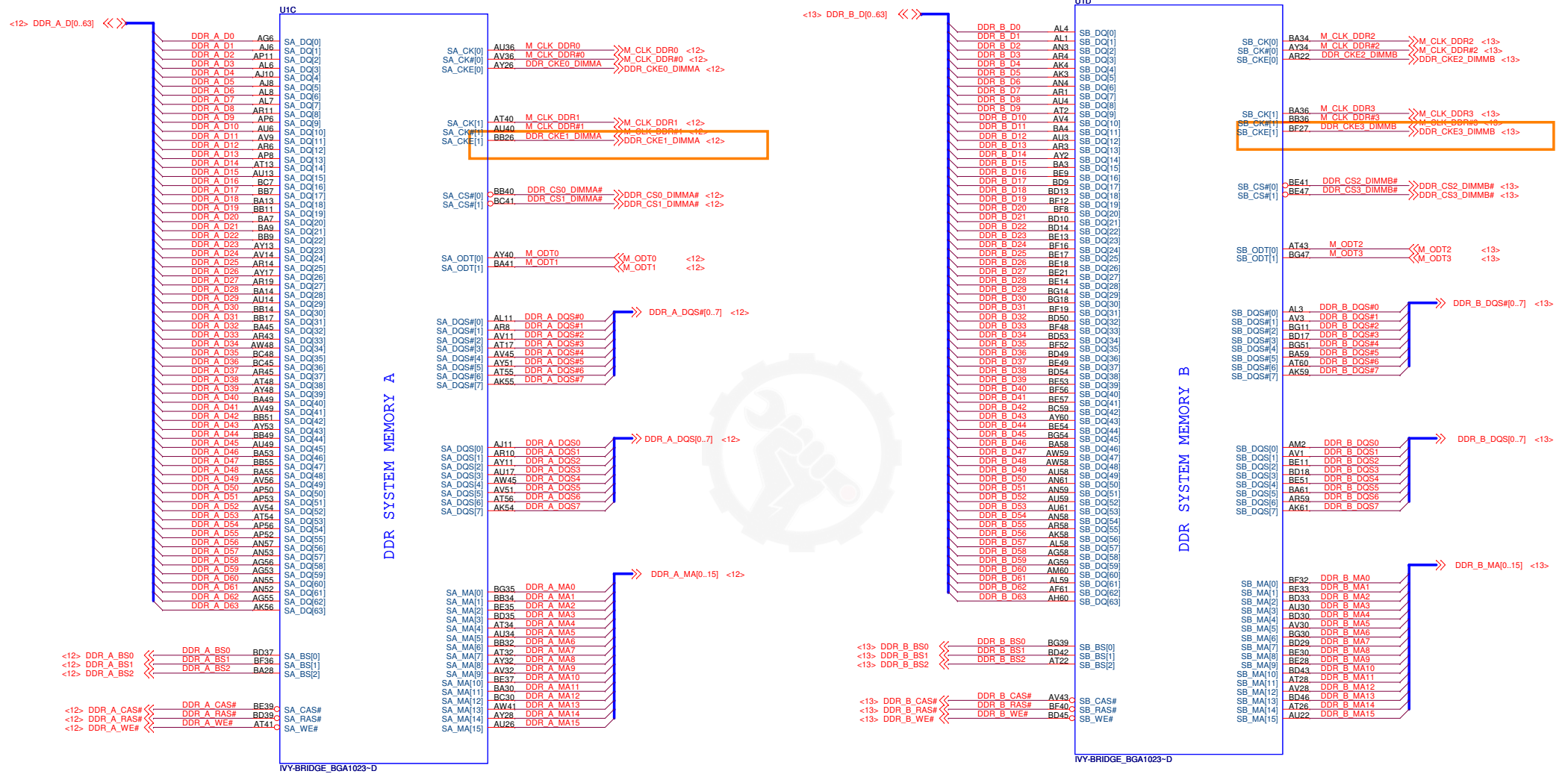
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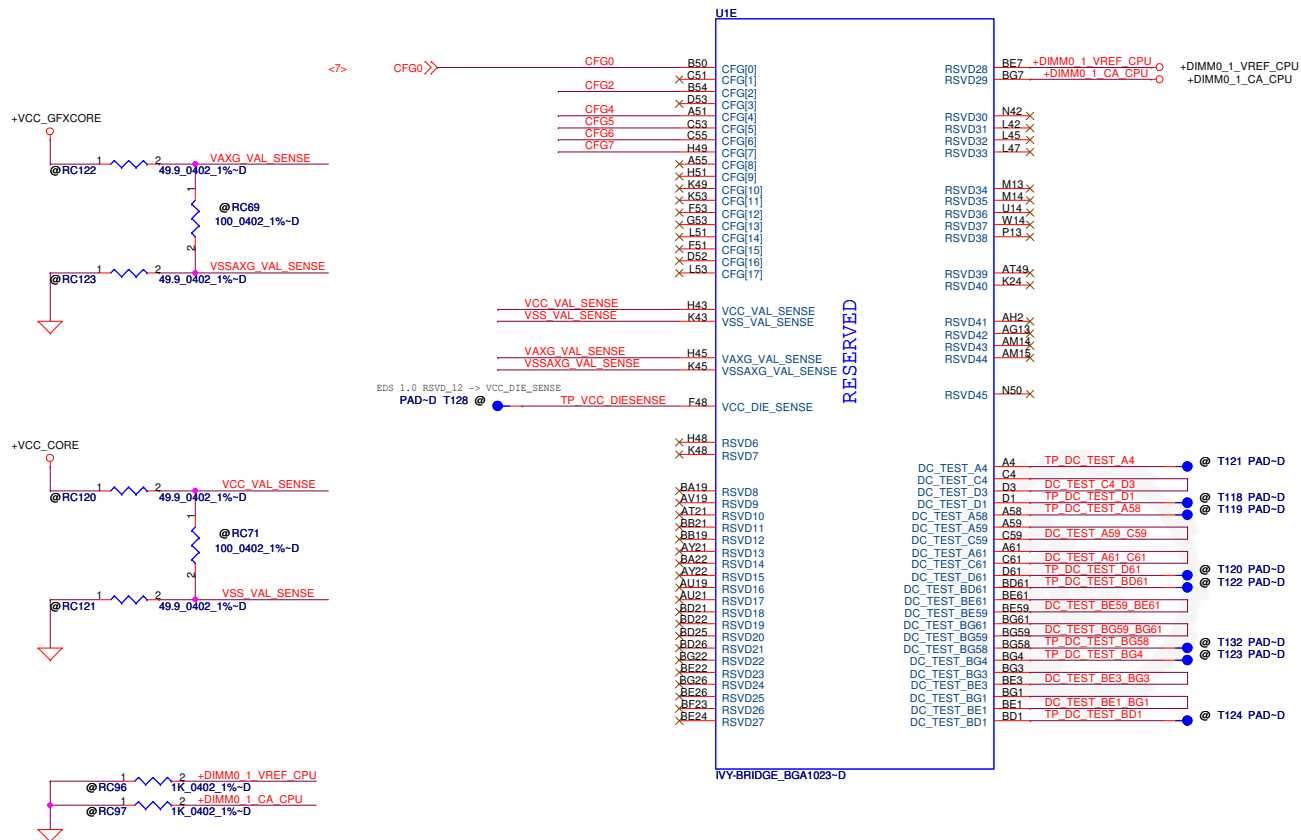


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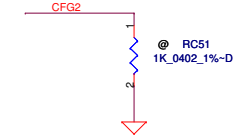
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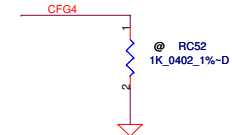




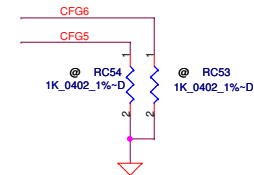
CFG Straps for Processor



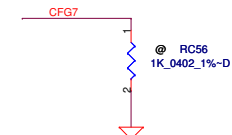
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training

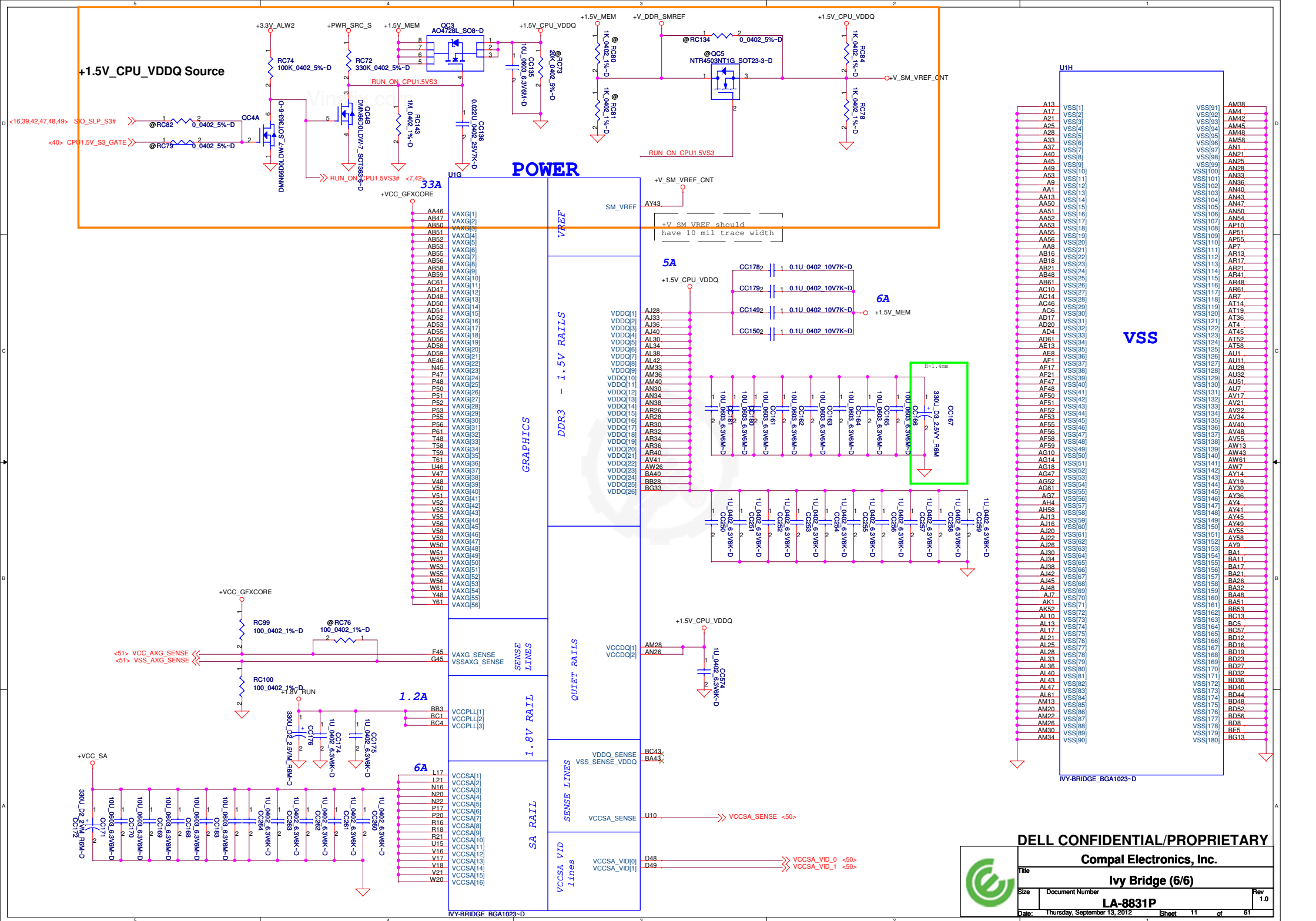
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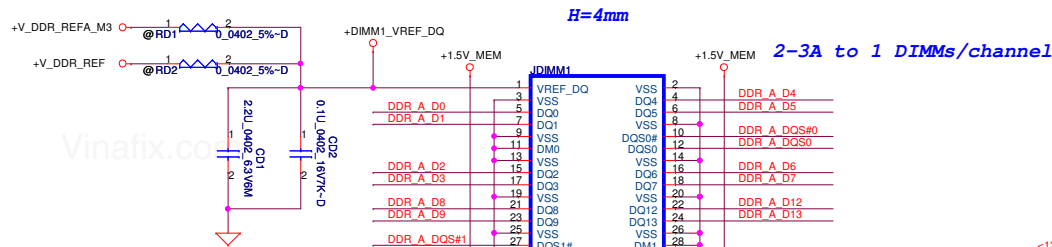
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Ivy Bridge (4/6)			
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Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

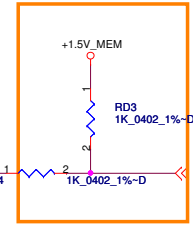
All VREF traces should have 10 mil trace width

<8> DDR_A_DQS#[0..7] <<>>
<8> DDR_A_D#[0..63] <<>>
<8> DDR_A_DQS#[0..7] <<>>
<8> DDR_A_MA#[0..15] <<>>

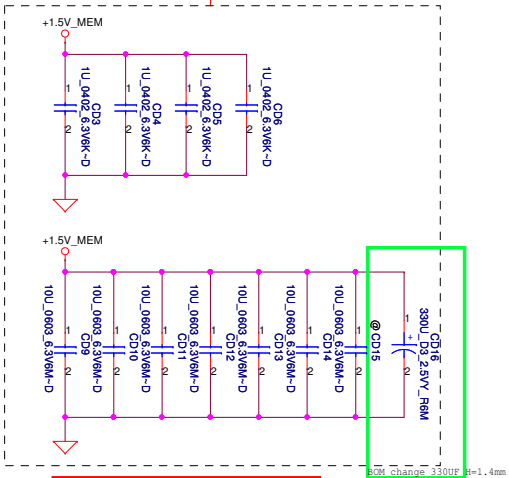
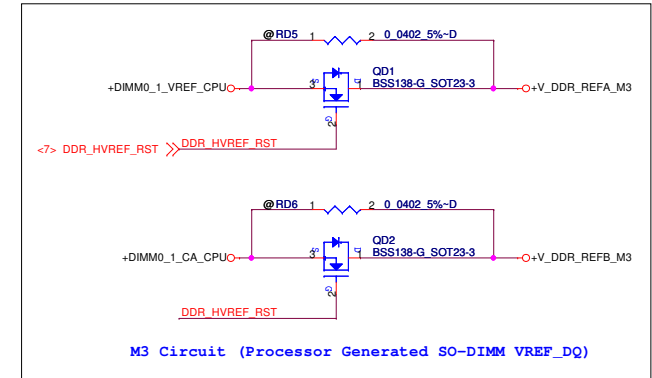
Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

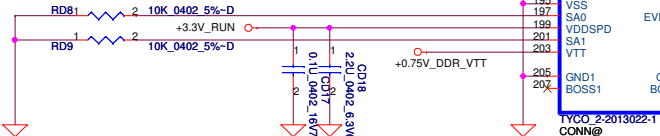
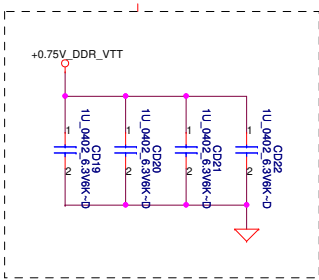
<8> DDR_CKE0_DIMMA <<>> DDR_CKE1_DIMMA <<>>
<8> DDR_A_BS2 <<>> DDR_CKE1_DIMMA <<>>
<8> M_CLK_DDR0 <<>> M_CLK_DDR1 <<>>
<8> M_CLK_DDR#0 <<>> M_CLK_DDR#1 <<>>
<8> DDR_A_BS0 <<>> DDR_A_BS1 <<>>
<8> DDR_A_WE# <<>> DDR_A_RAS# <<>>
<8> DDR_A_CAS# <<>> DDR_A_CAS# <<>>
<8> DDR_CS1_DIMMA# <<>> M_ODT0 <<>>
<8> M_ODT1 <<>> M_ODT1 <<>>



<13> DDR3_DRAMRST#_R <<>> DDR3_DRAMRST#_R <<>>
RD4



Layout Note:
Place near JDIMM1.203,204



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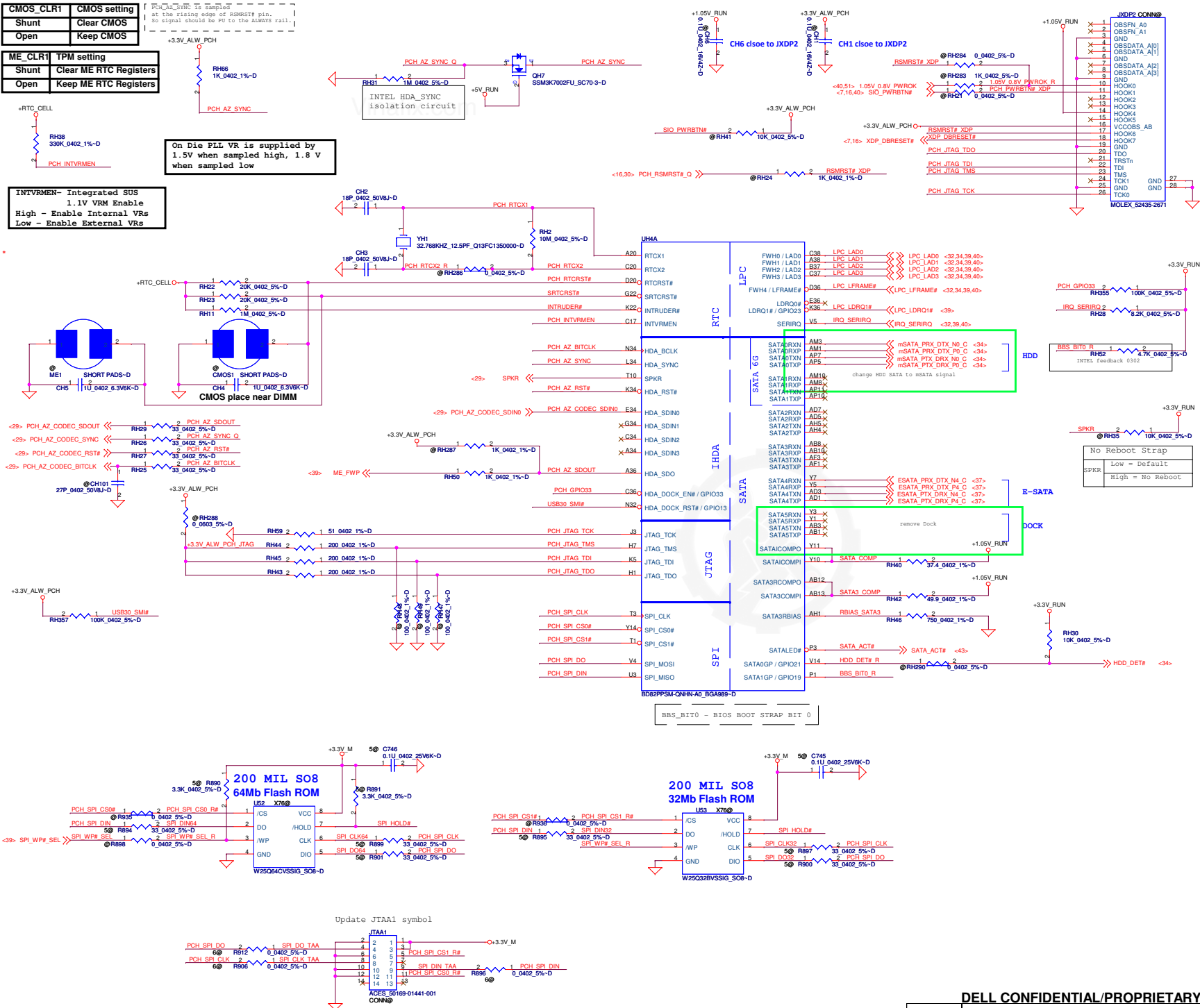
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DDRIII-SODIMM SLOT1			
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ME _{CLR1}	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

+RTC_CELL

On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

INTVRMEN- Integrated SUS
1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs



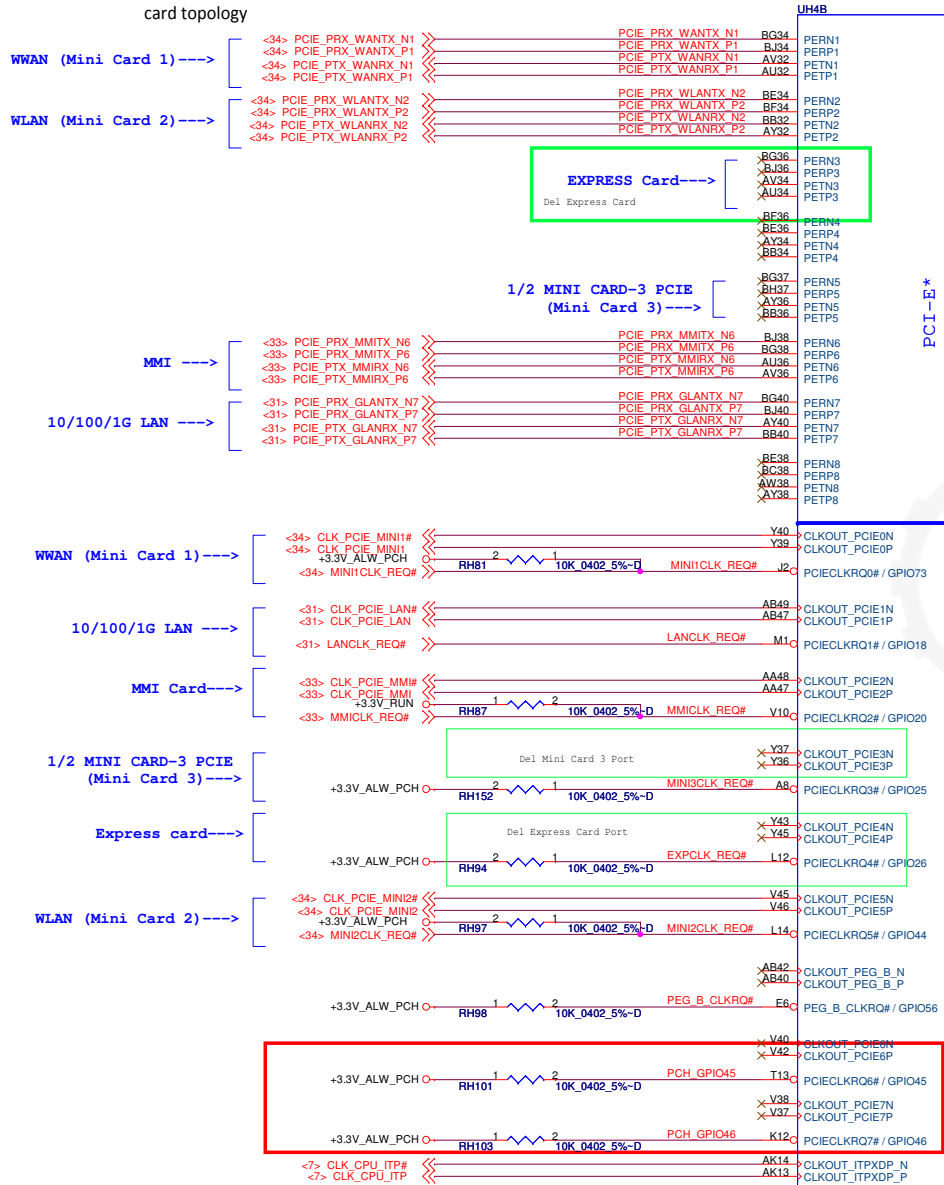
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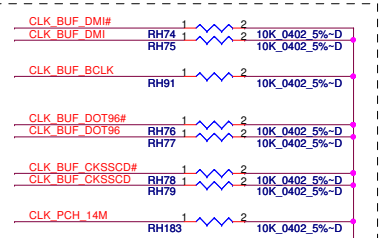
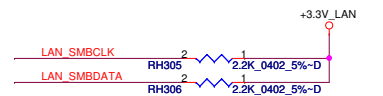
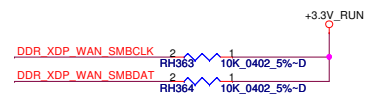
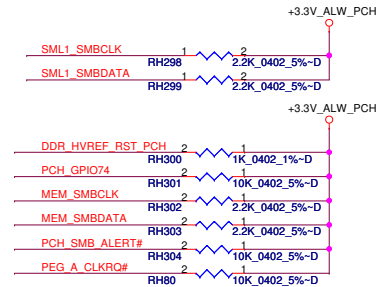
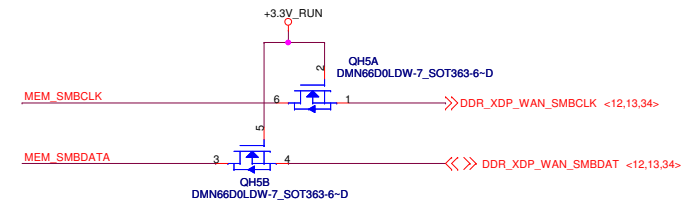
Follow DG0.9 Device
down & Express/Mini
card topology



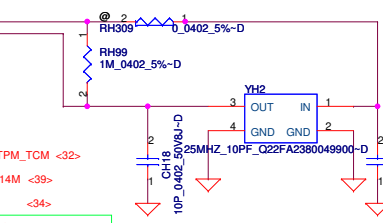
PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

RF request to add
CH112 close RH311

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CLOCK TERMINATION for FCIM and need close to PCH



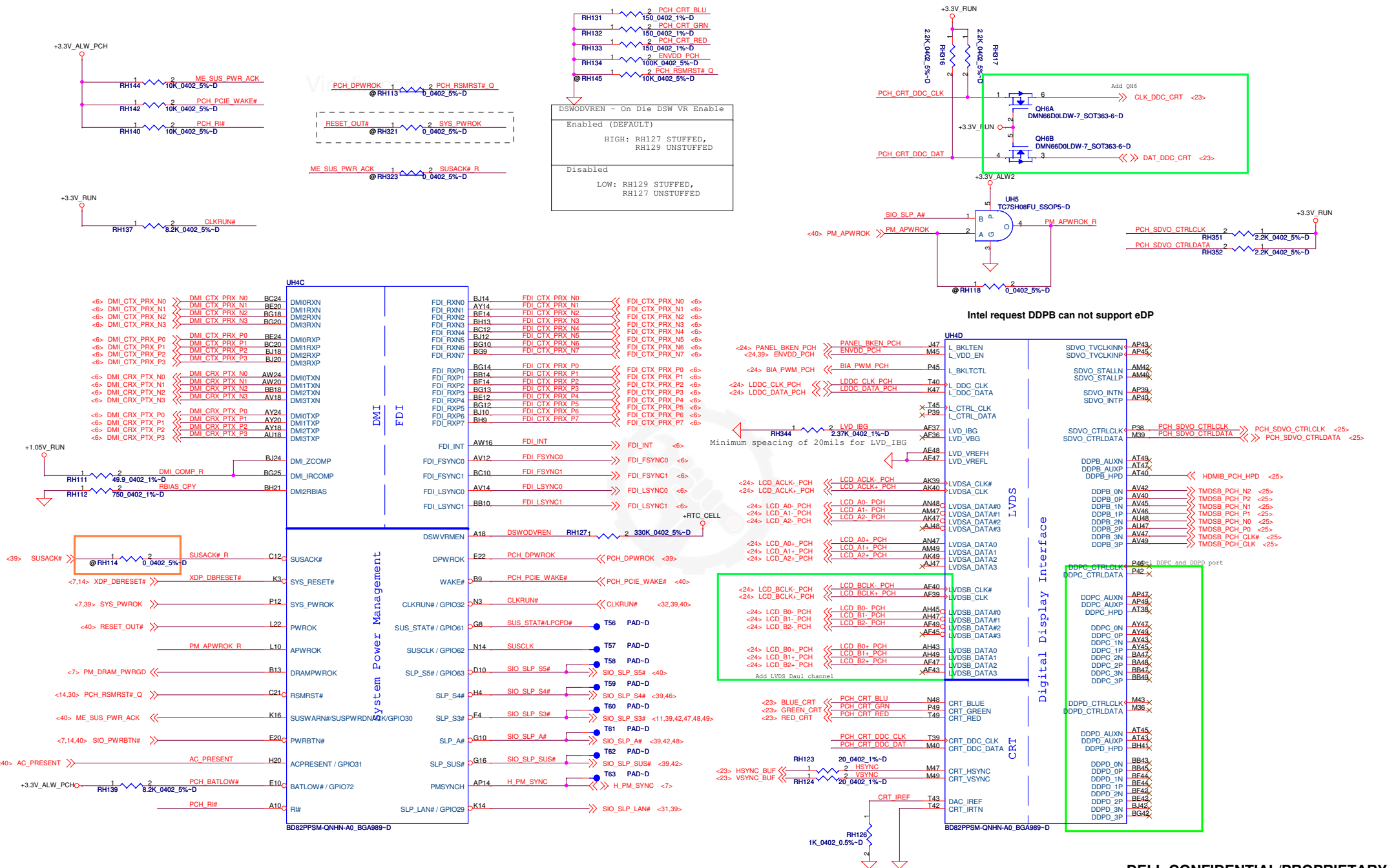
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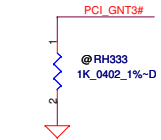
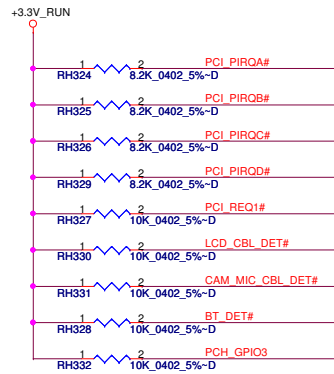
PCH (2/8)

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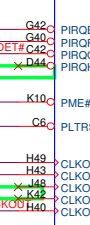
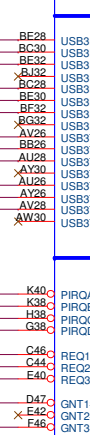
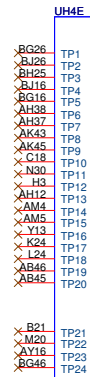
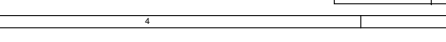
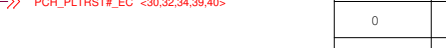
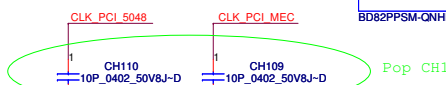
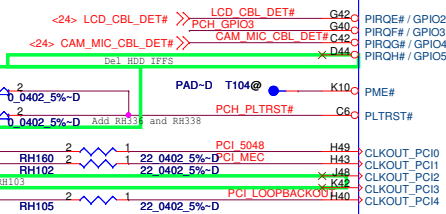
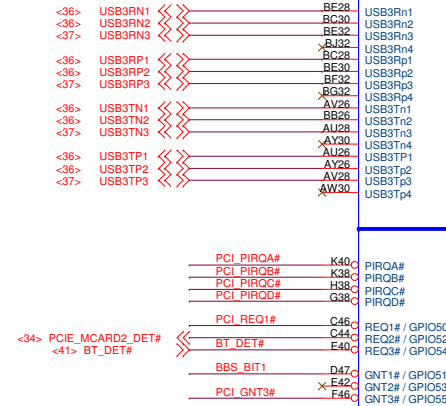
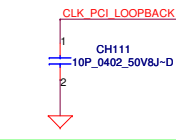
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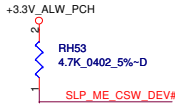


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

Remove RH335, RH336, RH337, RH338
to save room for D12" only

RF request to add
CH111 close RH105

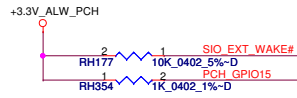




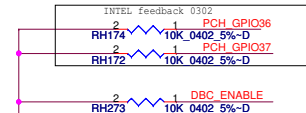
Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

SLP_ME_CSW_DEV# PLL ON DIE VR ENABLE

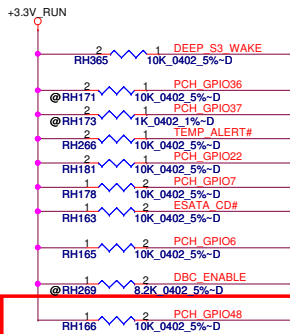
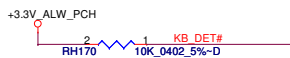
ENABLED - HIGH DEFAULT
DISABLED - LOW



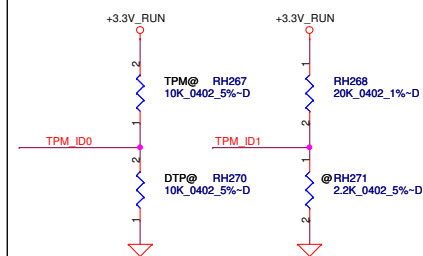
Intel feedback recommend 2.22



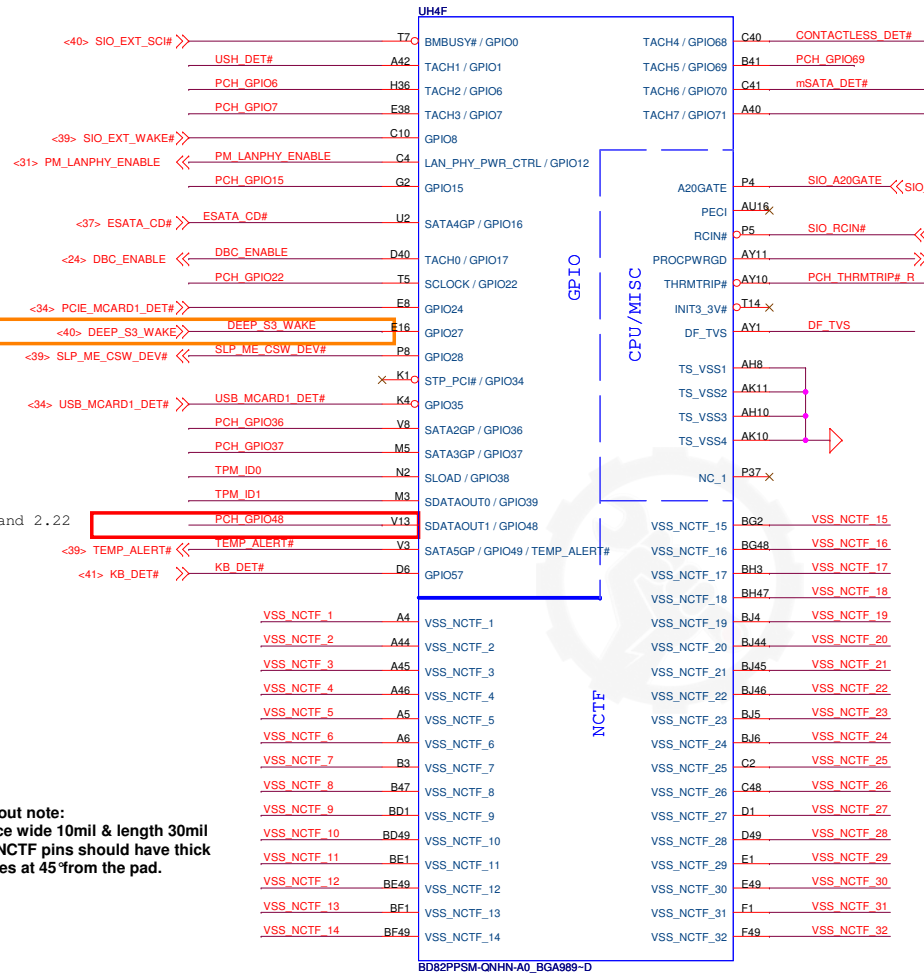
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



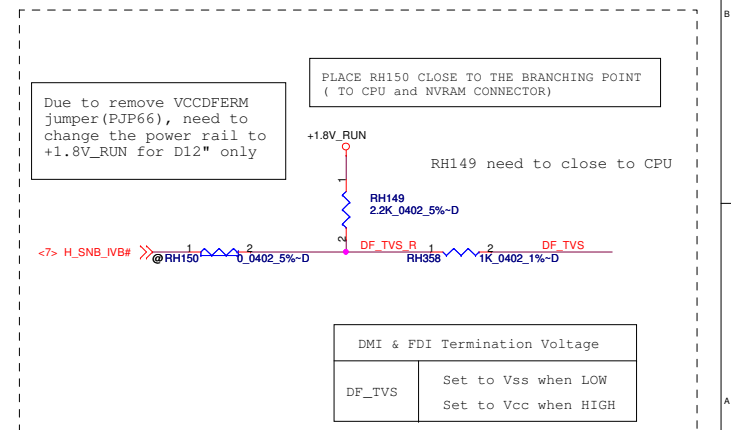
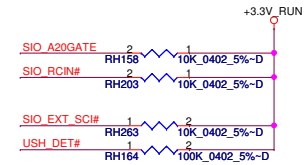
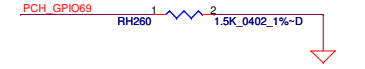
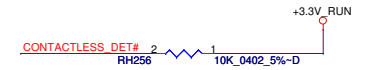
Intel feedback recommend 2.22



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1



Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



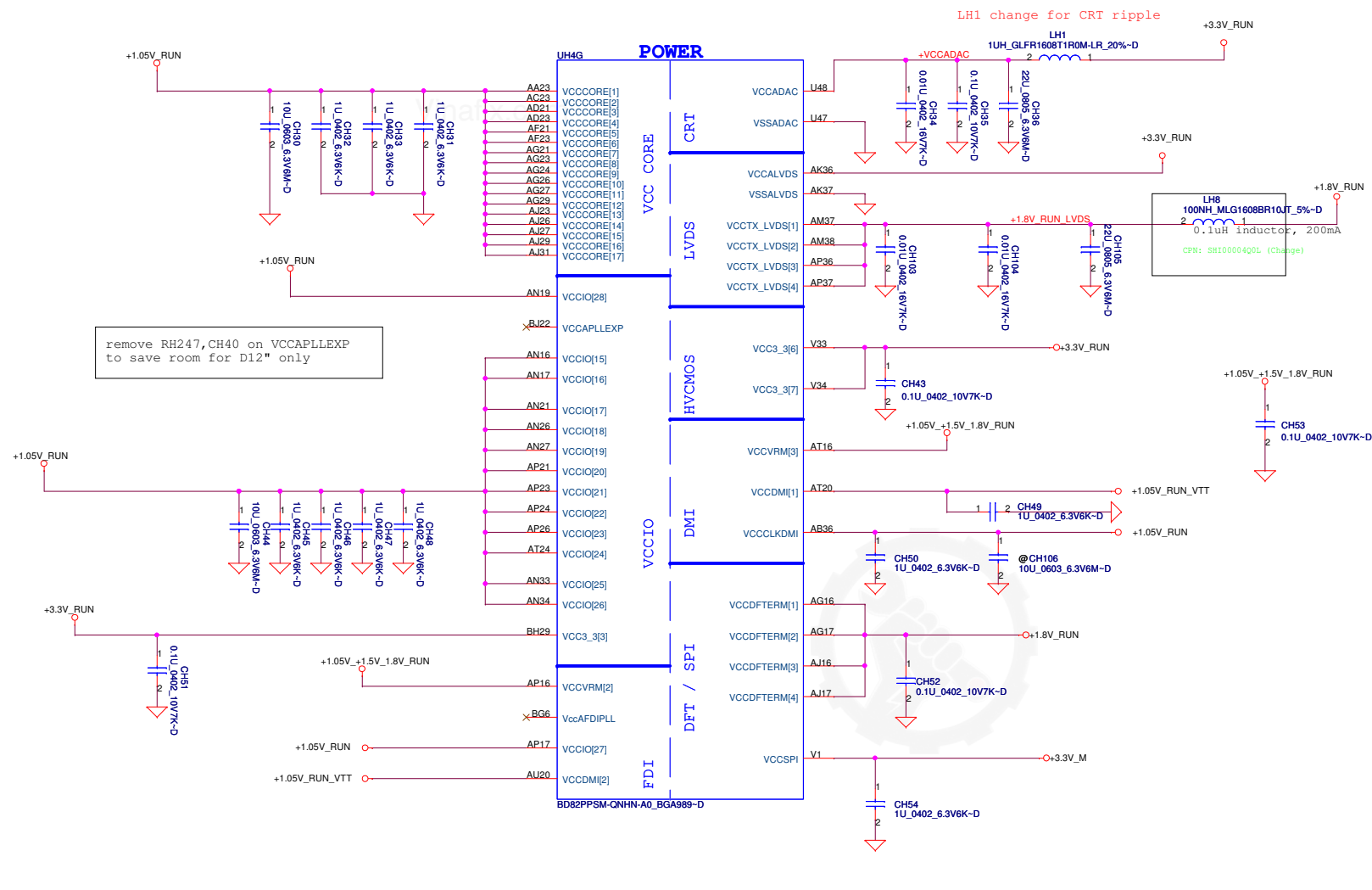
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PCH (5/8)

LA-8831P

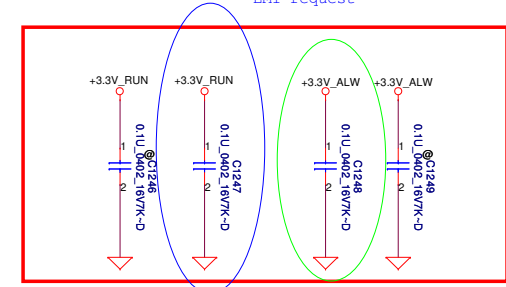
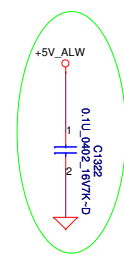
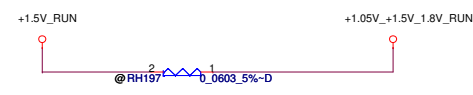
Date: Thursday, September 13, 2012 Sheet 18 of 61



PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.020
VccDSW3_3	3.3	0.003
VCCDFTerm	1.8	0.19
VccRTC	3.3	2 (mA)
VccSus3_3	3.3	0.119
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06
VccAPLEXP	1.05	0.05

RF request add C1248 and C1322 that close the PJP101 nad PJP103

EMI request



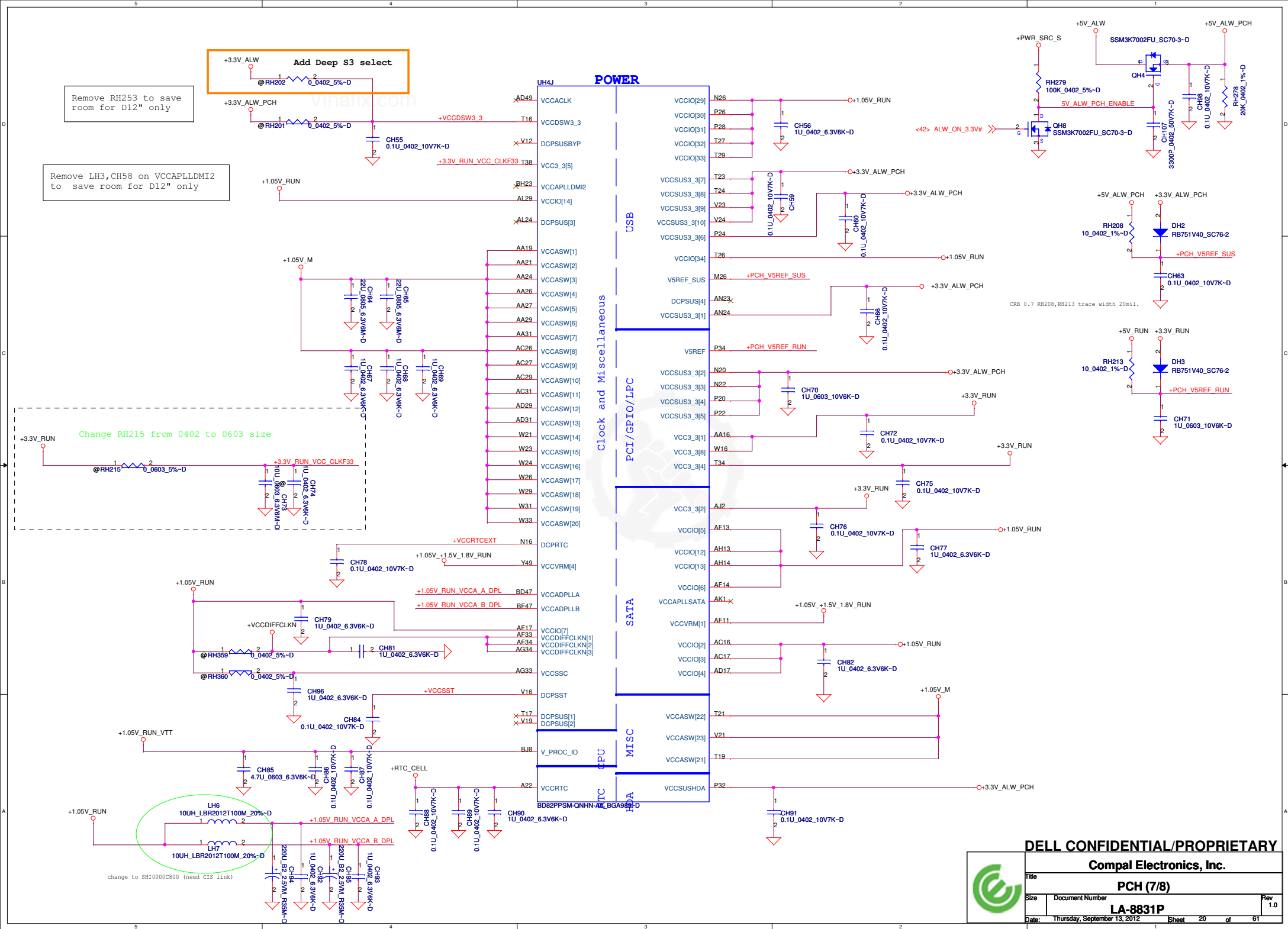
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UH4H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK46
AA33	VSS[4]	VSS[83] AK8
AA34	VSS[5]	VSS[84] AL16
AB11	VSS[6]	VSS[85] AL17
AB14	VSS[7]	VSS[86] AL19
AB39	VSS[8]	VSS[87] AL2
AB4	VSS[9]	VSS[88] AL21
AB43	VSS[10]	VSS[89] AL23
AB5	VSS[11]	VSS[90] AL26
AB7	VSS[12]	VSS[91] AL27
AC19	VSS[13]	VSS[92] AL31
AC2	VSS[14]	VSS[93] AL34
AC21	VSS[15]	VSS[94] AL48
AC24	VSS[16]	VSS[95] AM11
AC33	VSS[17]	VSS[96] AM14
AC34	VSS[18]	VSS[97] AM39
AC48	VSS[19]	VSS[98] AM43
AD10	VSS[20]	VSS[99] AM45
AD11	VSS[21]	VSS[100] AM7
AD12	VSS[22]	VSS[101] AN2
AD13	VSS[23]	VSS[102] AN29
AD24	VSS[24]	VSS[103] AN3
AD26	VSS[25]	VSS[104] AN31
AD27	VSS[26]	VSS[105] AP12
AD33	VSS[27]	VSS[106] AP19
AD34	VSS[28]	VSS[107] AP28
AD36	VSS[29]	VSS[108] AP32
AD37	VSS[30]	VSS[109] AP38
AD38	VSS[31]	VSS[110] AP4
AD39	VSS[32]	VSS[111] AP42
AD4	VSS[33]	VSS[112] AP46
AD40	VSS[34]	VSS[113] AP8
AD42	VSS[35]	VSS[114] AP8
AD43	VSS[36]	VSS[115] AR2
AD45	VSS[37]	VSS[116] AR48
AD46	VSS[38]	VSS[117] AT11
AD8	VSS[39]	VSS[118] AT13
AE2	VSS[40]	VSS[119] AT22
AE3	VSS[41]	VSS[120] AT26
AF10	VSS[42]	VSS[121] AT28
AF12	VSS[43]	VSS[122] AT30
AD14	VSS[44]	VSS[123] AT32
AD16	VSS[45]	VSS[124] AT34
AF16	VSS[46]	VSS[125] AT39
AF19	VSS[47]	VSS[126] AT42
AF24	VSS[48]	VSS[127] AT46
AF26	VSS[49]	VSS[128] AU24
AF27	VSS[50]	VSS[129] AU30
AF29	VSS[51]	VSS[130] AV16
AF31	VSS[52]	VSS[131] AV20
AF38	VSS[53]	VSS[132] AV24
AF4	VSS[54]	VSS[133] AV30
AF42	VSS[55]	VSS[134] AV38
AF5	VSS[56]	VSS[135] AV4
AF7	VSS[57]	VSS[136] AV8
AF8	VSS[58]	VSS[137] AW14
AG19	VSS[59]	VSS[138] AW18
AG2	VSS[60]	VSS[139] AW2
AG3	VSS[61]	VSS[140] AW22
AG31	VSS[62]	VSS[141] AW26
AG48	VSS[63]	VSS[142] AW28
AH11	VSS[64]	VSS[143] AW32
AH3	VSS[65]	VSS[144] AW36
AH36	VSS[66]	VSS[145] AW40
AH39	VSS[67]	VSS[146] AW44
AH40	VSS[68]	VSS[147] AW48
AH42	VSS[69]	VSS[148] AW52
AH46	VSS[70]	VSS[149] AW56
AH7	VSS[71]	VSS[150] AW60
AJ19	VSS[72]	VSS[151] AW64
AJ21	VSS[73]	VSS[152] AW68
AJ24	VSS[74]	VSS[153] AW72
AJ33	VSS[75]	VSS[154] AW76
AJ34	VSS[76]	VSS[155] AW80
AK12	VSS[77]	VSS[156] AW84
AK3	VSS[78]	VSS[157] AW88
	VSS[79]	VSS[158] AW92

BD82PPSM-QNHN-A0_BGA989-D

UH4I

AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B39	VSS[169]	VSS[269] L38
B7	VSS[170]	VSS[270] L48
F45	VSS[171]	VSS[271] M12
B12	VSS[172]	VSS[272] M18
BB16	VSS[173]	VSS[273] M22
BB20	VSS[174]	VSS[274] M24
BB22	VSS[175]	VSS[275] M30
BB24	VSS[176]	VSS[276] M32
BB28	VSS[177]	VSS[277] M34
BB30	VSS[178]	VSS[278] M38
BB38	VSS[179]	VSS[279] M4
BB4	VSS[180]	VSS[280] M42
BB46	VSS[181]	VSS[281] M46
BC14	VSS[182]	VSS[282] M8
BC18	VSS[183]	VSS[283] N18
BC2	VSS[184]	VSS[284] N24
BC22	VSS[185]	VSS[285] N30
BC26	VSS[186]	VSS[286] N34
BC32	VSS[187]	VSS[287] P11
BC34	VSS[188]	VSS[288] P18
BC36	VSS[189]	VSS[289] P40
BC40	VSS[190]	VSS[290] P43
BC42	VSS[191]	VSS[291] P47
BC48	VSS[192]	VSS[292] P7
BD46	VSS[193]	VSS[293] R2
BD5	VSS[194]	VSS[294] R48
BE22	VSS[195]	VSS[295] T12
BE26	VSS[196]	VSS[296] T3
BE40	VSS[197]	VSS[297] T4
BF10	VSS[198]	VSS[298] W34
BF12	VSS[199]	VSS[299] T46
BF16	VSS[200]	VSS[300] T8
BF20	VSS[201]	VSS[301] V11
BF22	VSS[202]	VSS[302] V17
BF24	VSS[203]	VSS[303] V26
BF26	VSS[204]	VSS[304] V27
BF28	VSS[205]	VSS[305] V29
BF48	VSS[206]	VSS[306] V31
BF8	VSS[207]	VSS[307] V38
BF30	VSS[208]	VSS[308] W17
BF38	VSS[209]	VSS[309] W19
BF40	VSS[210]	VSS[310] W2
BF8	VSS[211]	VSS[311] W27
BG17	VSS[212]	VSS[312] W48
BG21	VSS[213]	VSS[313] Y12
BG33	VSS[214]	VSS[314] Y4
BG44	VSS[215]	VSS[315] Y42
BG8	VSS[216]	VSS[316] Y8
BH11	VSS[217]	VSS[317] BG29
BH15	VSS[218]	VSS[318] N24
BH17	VSS[219]	VSS[319] A3
BH19	VSS[220]	VSS[320] AD47
H10	VSS[221]	VSS[321] B43
BH27	VSS[222]	VSS[322] BE10
BH31	VSS[223]	VSS[323] BG41
BH33	VSS[224]	VSS[324] G14
BH35	VSS[225]	VSS[325] H16
BH39	VSS[226]	VSS[326] T36
BH43	VSS[227]	VSS[327] BG22
BH7	VSS[228]	VSS[328] BG24
D3	VSS[229]	VSS[329] C22
D12	VSS[230]	VSS[330] AP13
D16	VSS[231]	VSS[331] M14
D18	VSS[232]	VSS[332] AP3
D22	VSS[233]	VSS[333] AP1
D24	VSS[234]	VSS[334] BE16
D26	VSS[235]	VSS[335] BC16
D30	VSS[236]	VSS[336] BG28
D32	VSS[237]	VSS[337] B28
D34	VSS[238]	VSS[338] F3
D38	VSS[239]	
D42	VSS[240]	
D8	VSS[241]	
E18	VSS[242]	
F26	VSS[243]	
G18	VSS[244]	
G20	VSS[245]	
G26	VSS[246]	
G28	VSS[247]	
G36	VSS[248]	
G48	VSS[249]	
H12	VSS[250]	
H18	VSS[251]	
H22	VSS[252]	
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

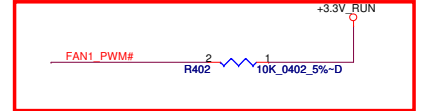
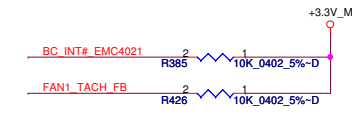
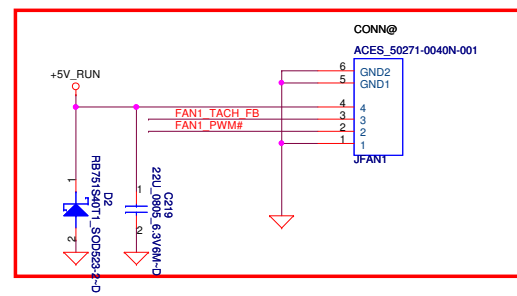
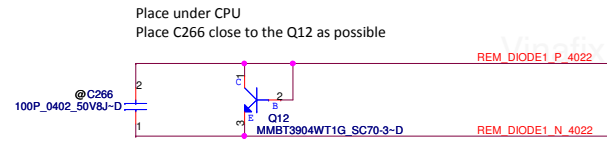
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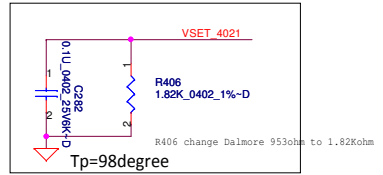
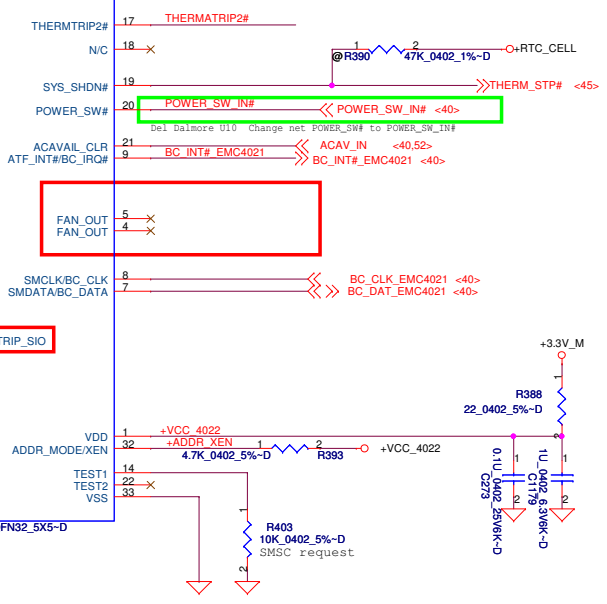
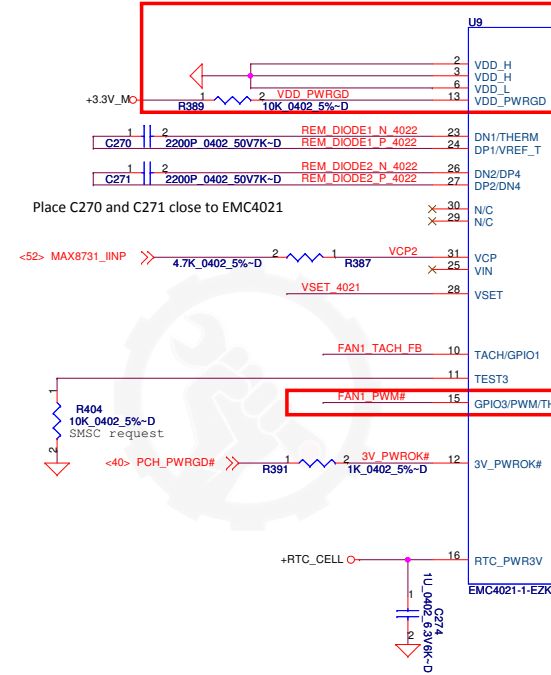
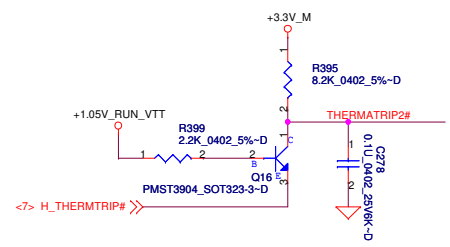
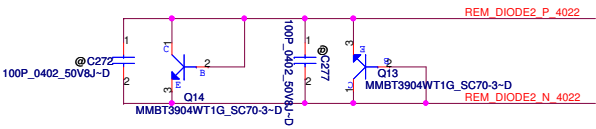
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- (1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
(2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke. Pleas and C277 close to Q13



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FAN & Thermal Sensor			
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ESD ask to add D77, D83

fix.com

Compal P/N SM01000FH0L
BLM15BB470SN1D (MURATA)

<16> RED_CRT

<16> GREEN_CRT

<16> BLUE_CRT

D77 and D83
change to de-pop (ESD suggest) 7/6

Del U18 for CRT Docking Switch

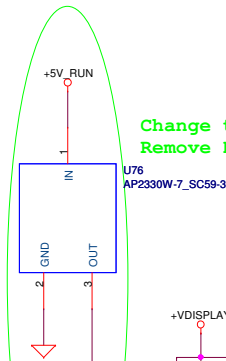
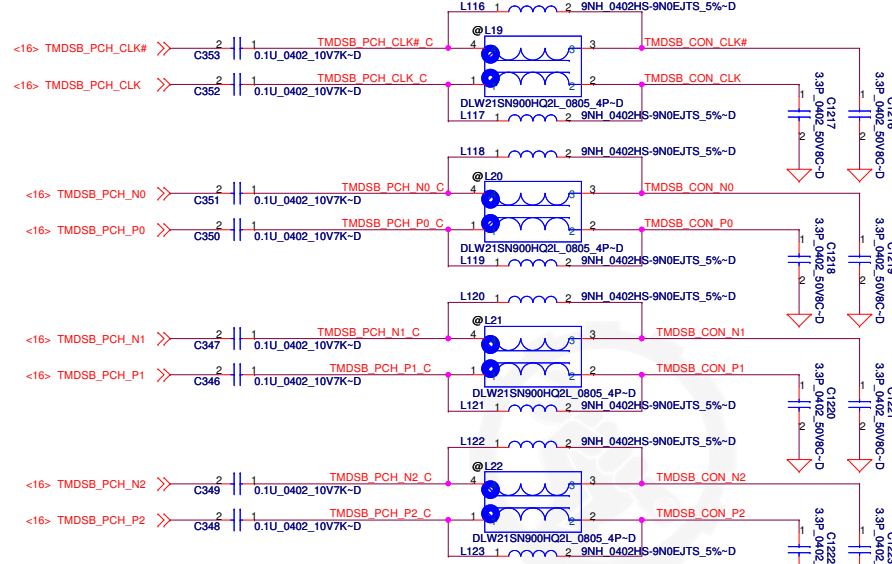
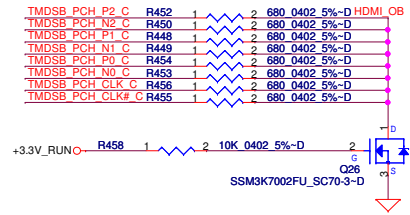
<16> DAT_DDC_CRT
<16> CLK_DDC_CRT

Change to 0402 size

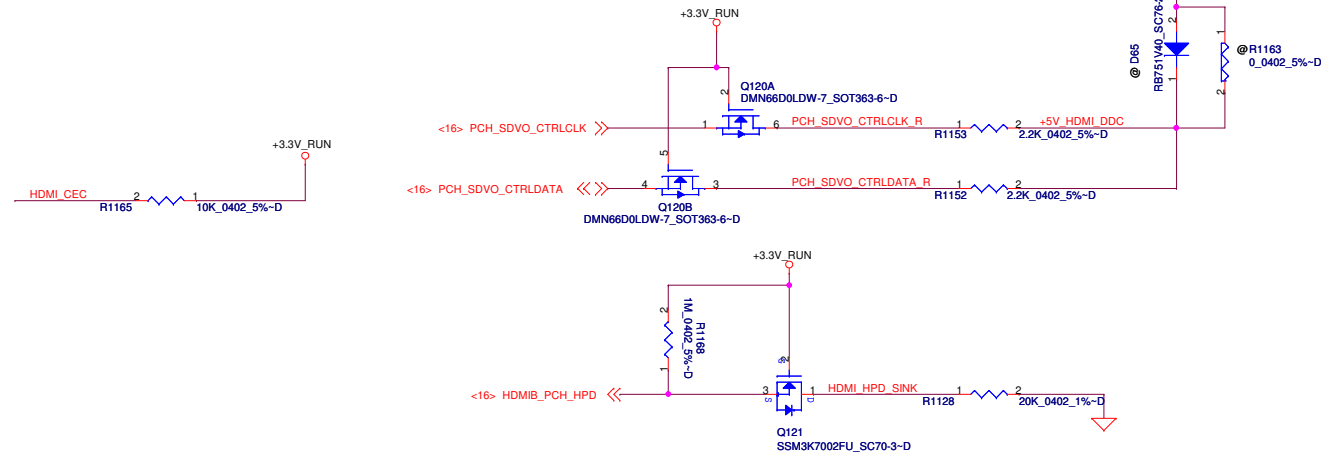
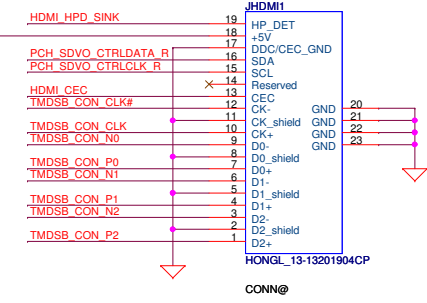
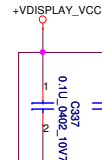
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CRT			
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EMI solution. Pop L116~L123, de-pop L19~L22



Change to new solution (U76)
Remove Diode and Fuse



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Vinafix.com


Del U20,U21,U23,U24 Dock function

BLANK



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Title		DP AUX SW	
Size	Document Number	Rev	
	LA-8831P	1.0	
Date: Thursday, September 13, 2012		Sheet	26 of 61

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Del HDD Function u88 and JSATA1



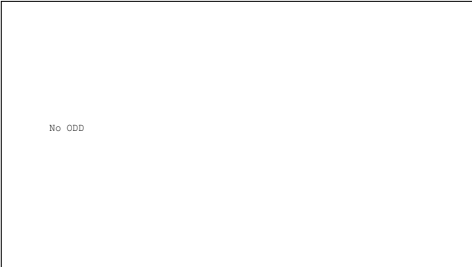
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Title		HDD CONNECTOR	
Size	Document Number	Rev	1.0
Date: Thursday, September 13, 2012		Sheet	27 of 61

Vinafix.com

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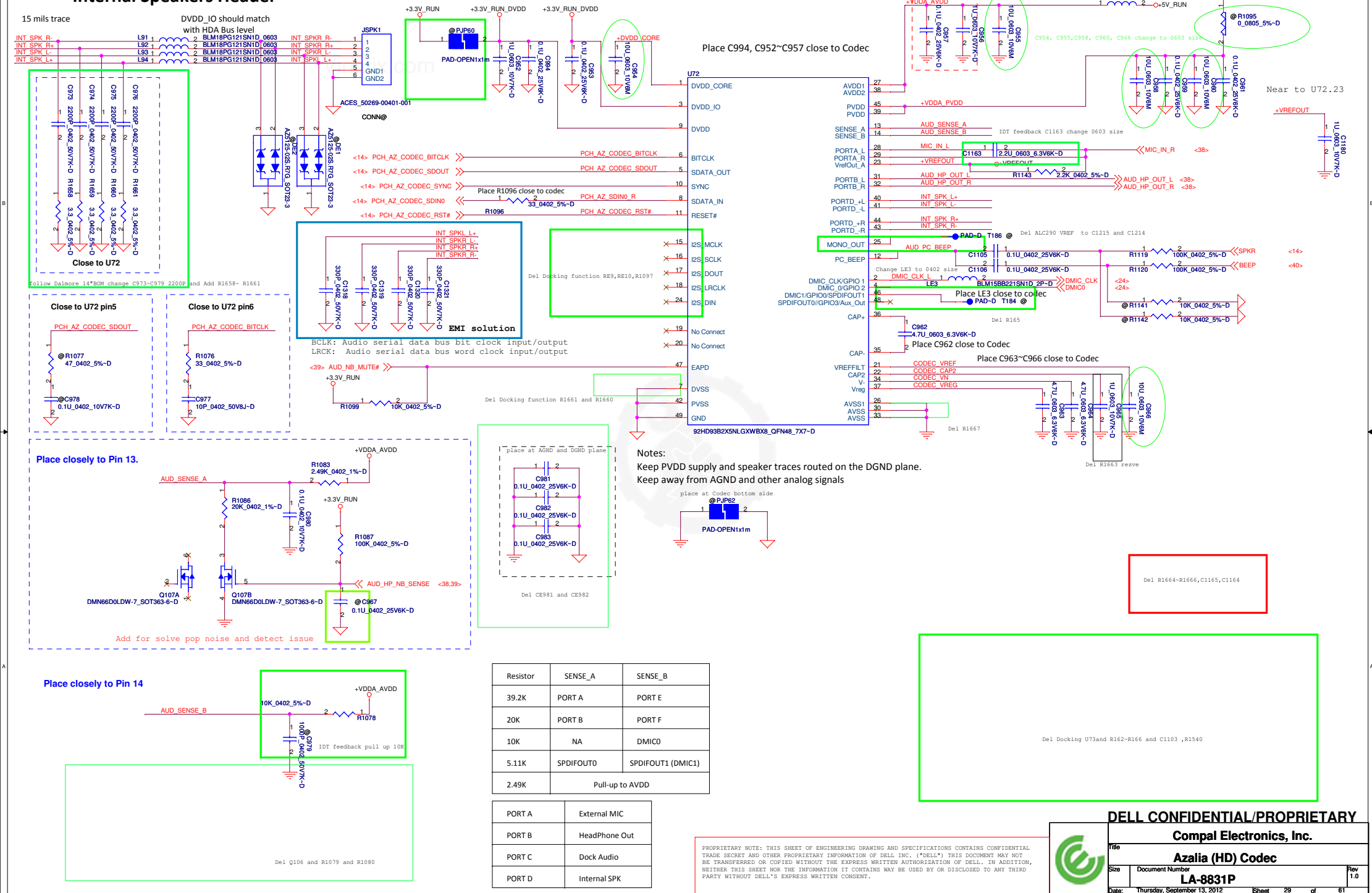


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Title			BRANK		
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Internal Speakers Header



Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

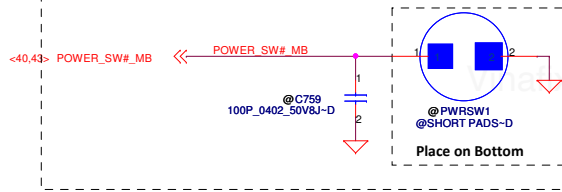
PORT A	External MIC
PORT B	HeadPhone Out
PORT C	Dock Audio
PORT D	Internal SPK

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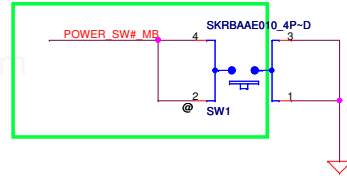


DELL CONFIDENTIAL/PROPRIETARY			
Compal Electronics, Inc.			
Title			
Azalia (HD) Codec			
Size	Document Number		Rev
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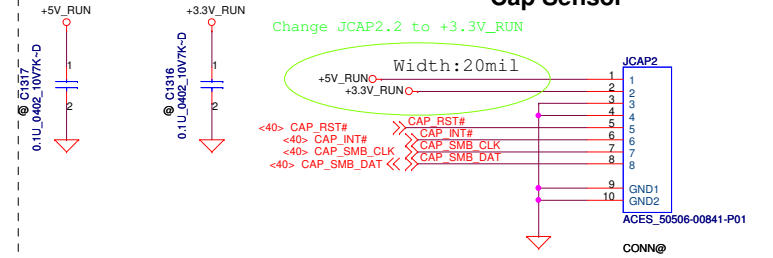
Power Switch for debug



Reserve for debugging (X-build will remove)
Change to E3 use part (SN11100580L)

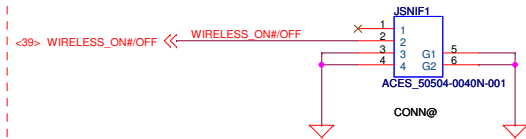


Cap Sensor



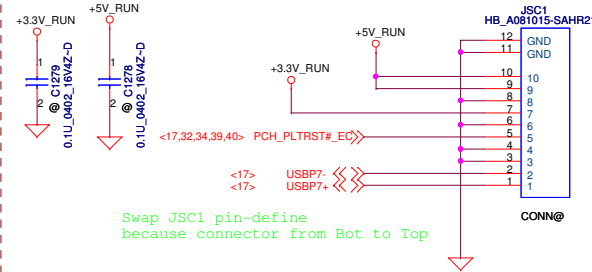
Default on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

Sniffer



Smart Card

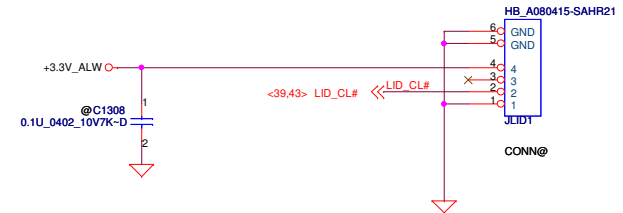
Change JLI1 connector to HB_A081015-SAHR21



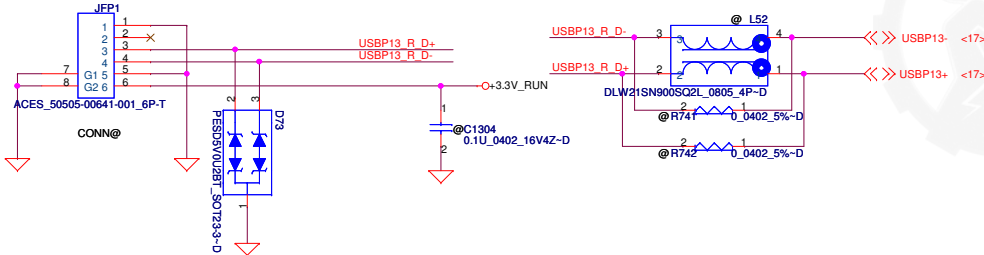
Lid board

Swap JLI1 pin-define
because connector from Bot to Top

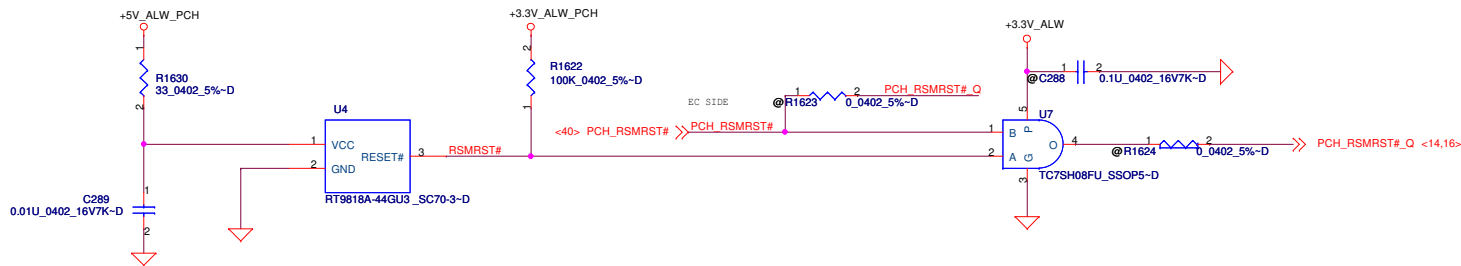
Change JLI1 connector to HB_A080415-SAHR21



Fingerprint CONN.



RSMRST circuit

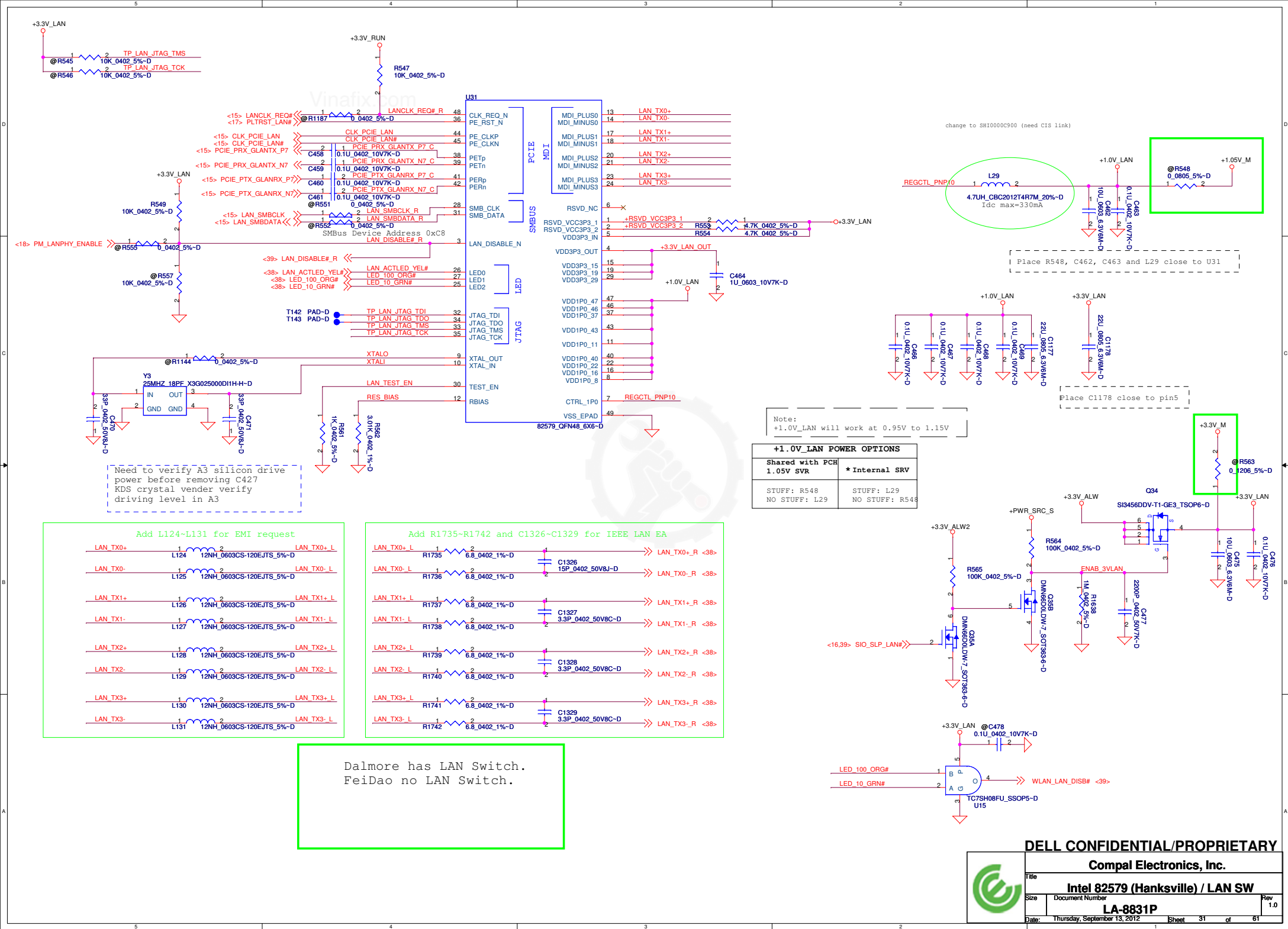


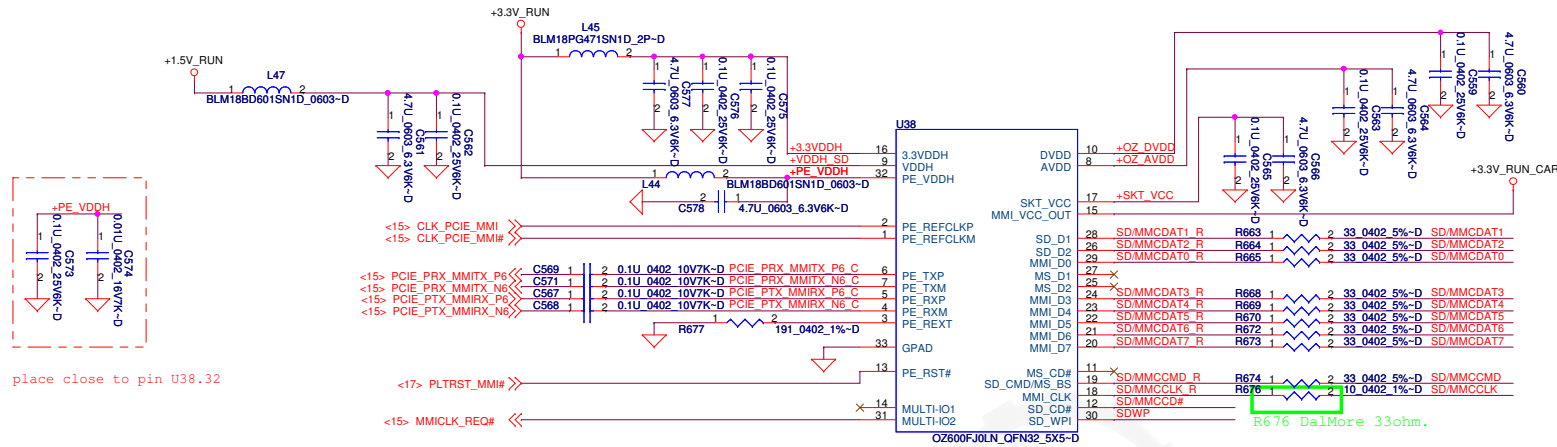
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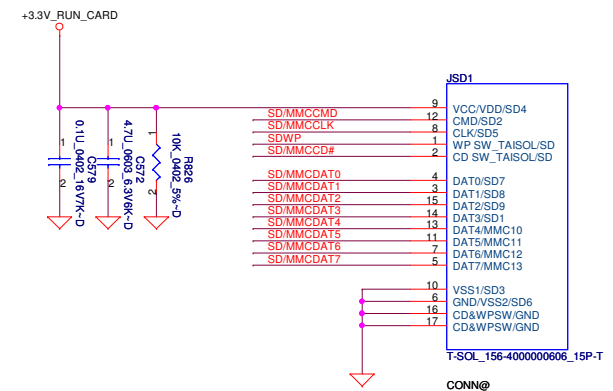
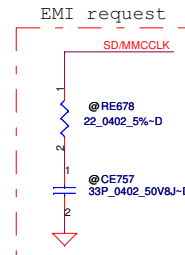
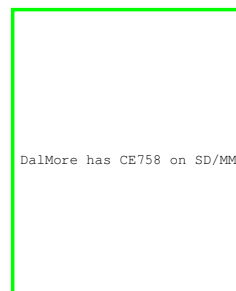
Title			
PWR SW/Sub-board Connector			
Size	Document Number		Rev
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Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible



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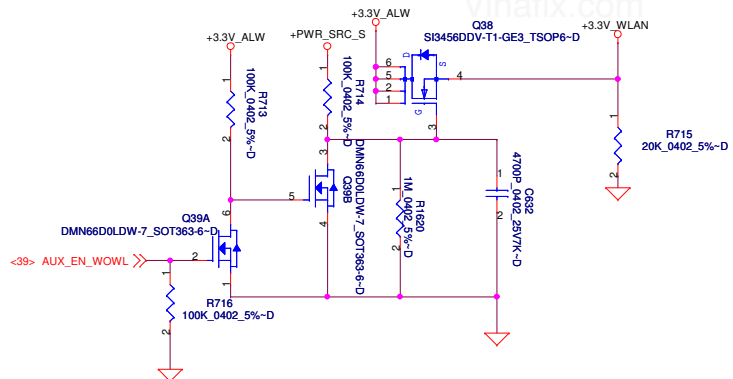
Card Reader OZ600FJ0

LA-8831P

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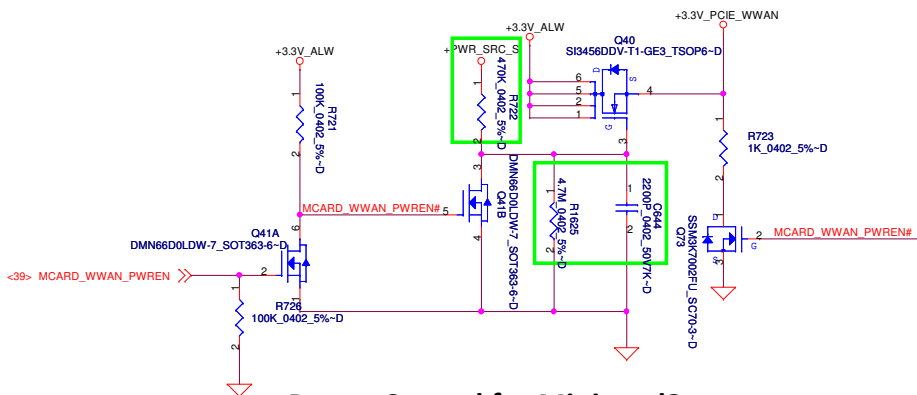
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Power Control for Mini card2

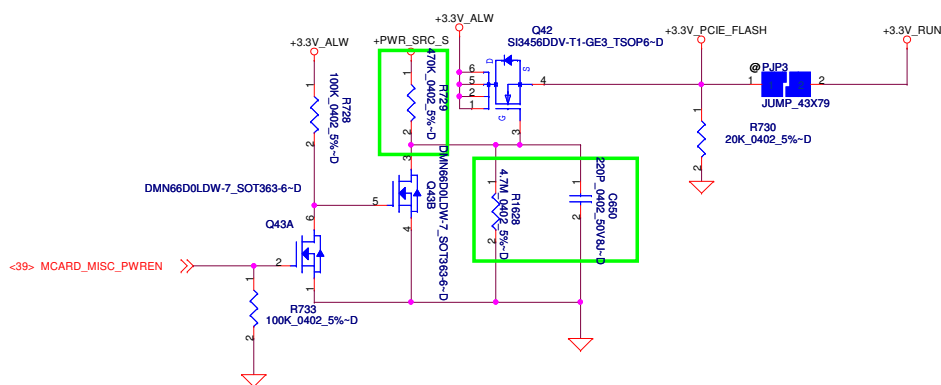


DalMore has ExprssCard PWR/Connector.

Power Control for Mini card1



Power Control for Mini card3

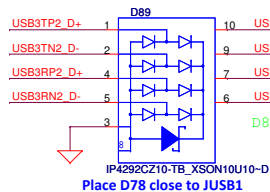
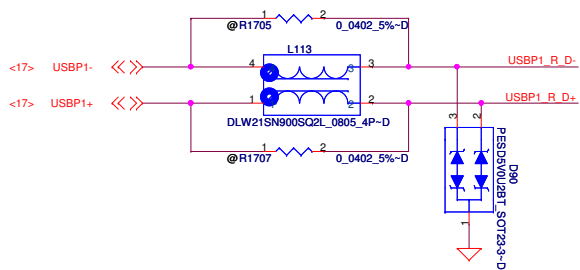
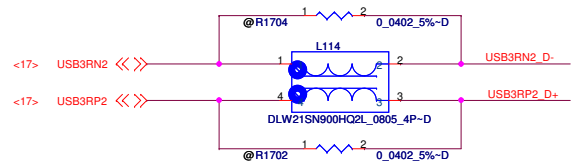
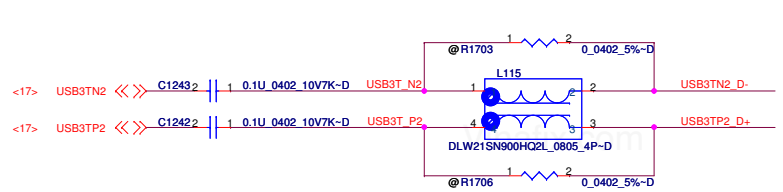


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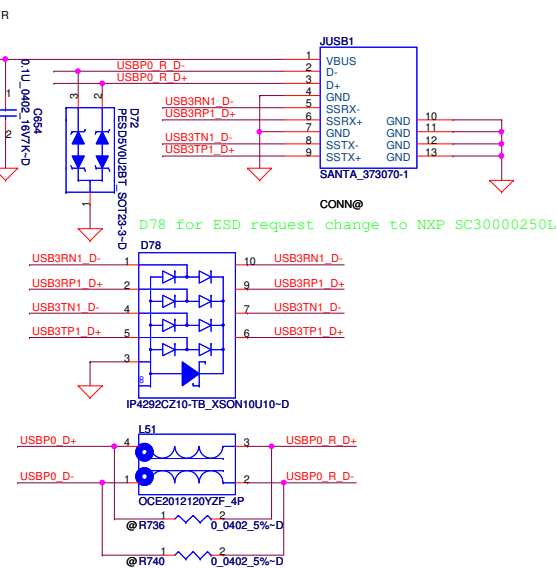
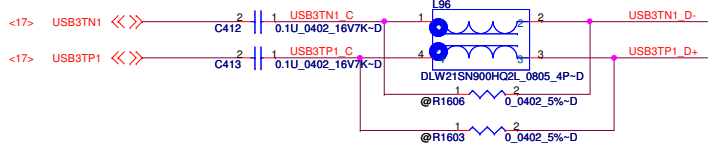
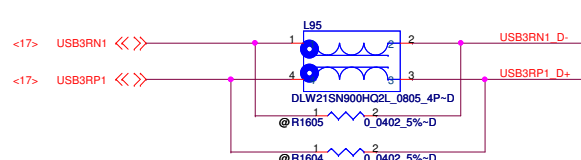
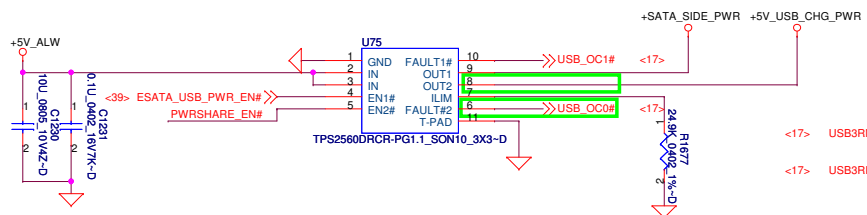
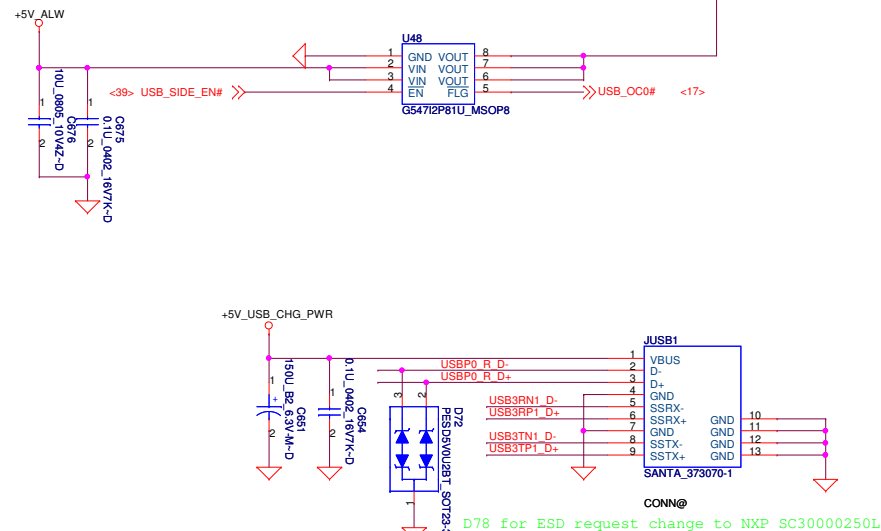
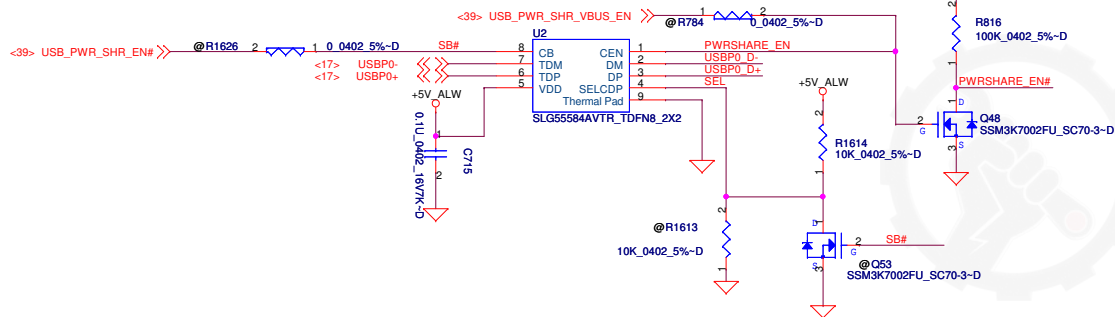
Title			
PCIE-SATA SW / PCIE PWR			
Size	Document Number	Rev	
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Place D72 close to JUSB1

D79 for ESD request change to NXP SC30000250L

SA00004VH00 (SLG55584) CIS Link OK



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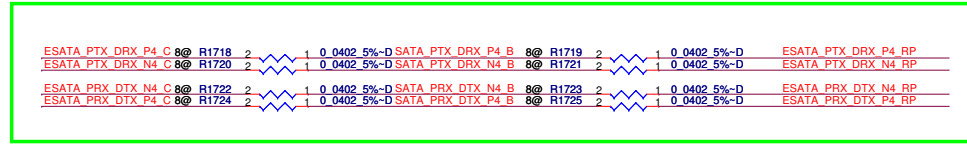
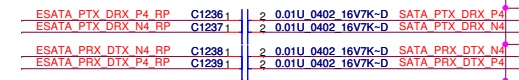
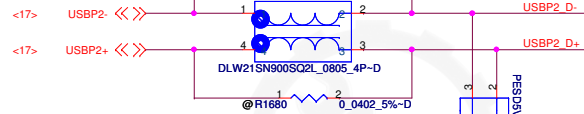
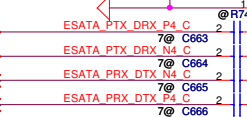
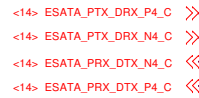
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USB 3.0

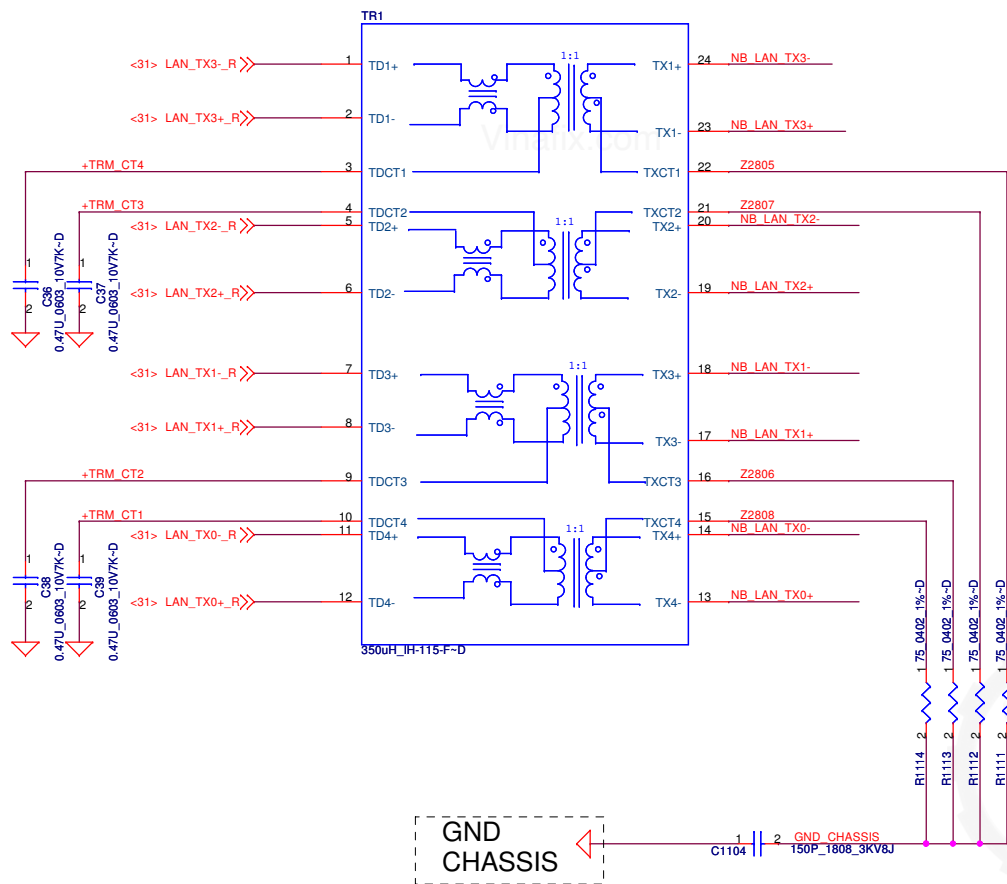
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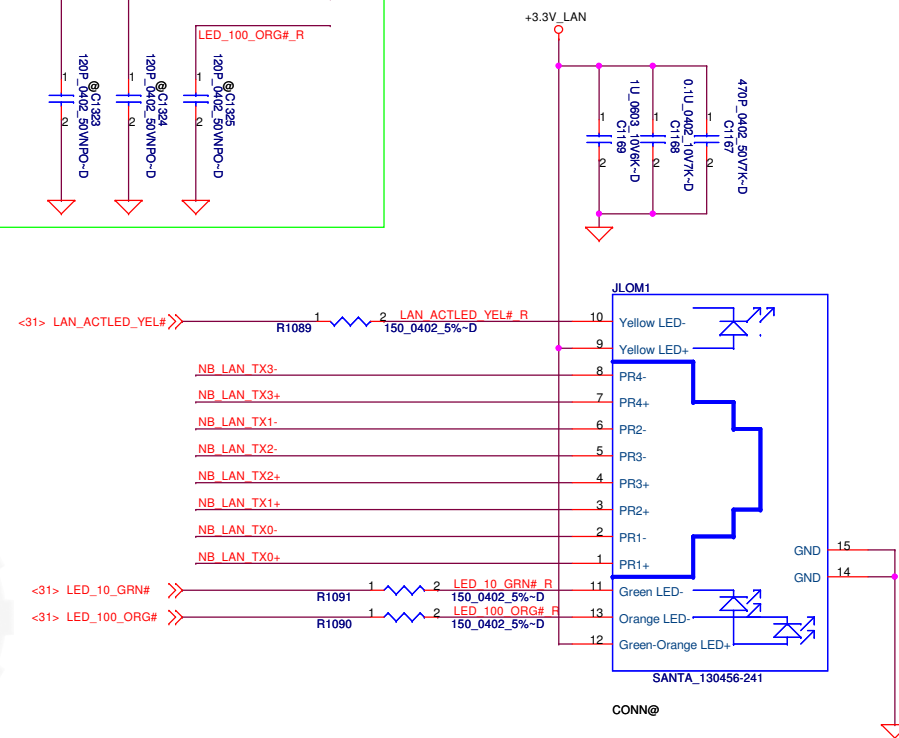
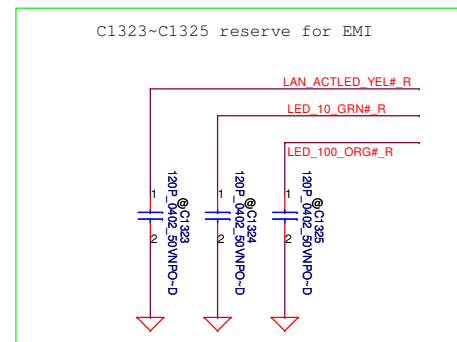
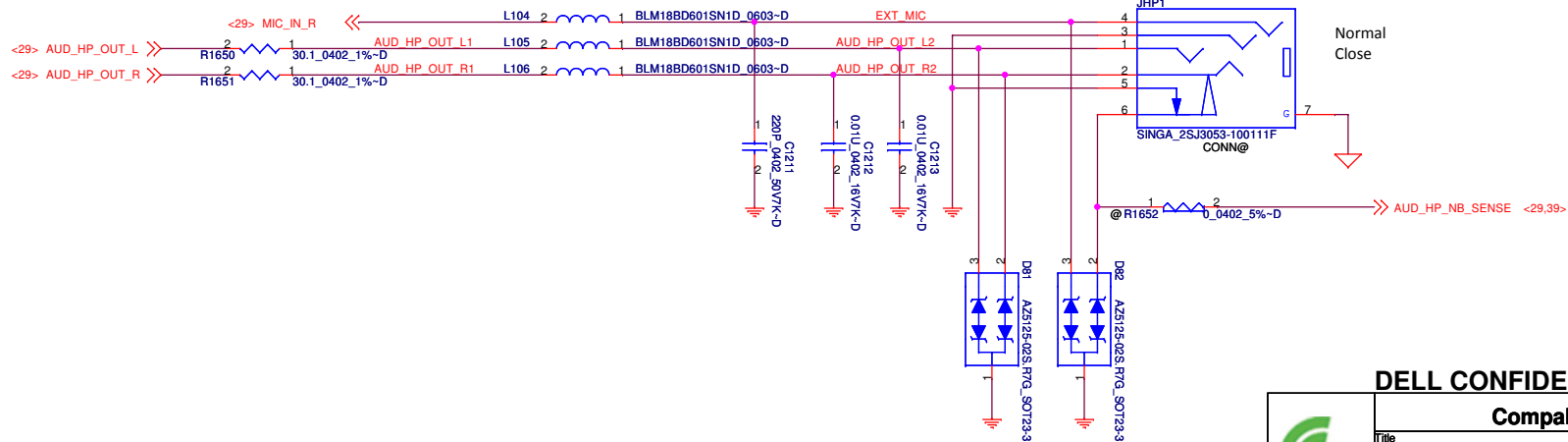
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Combo Jack

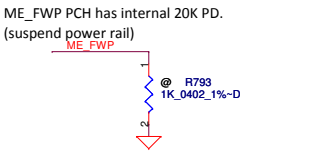
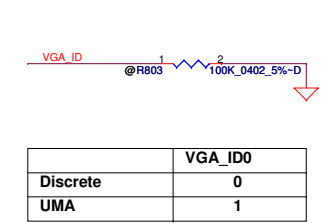
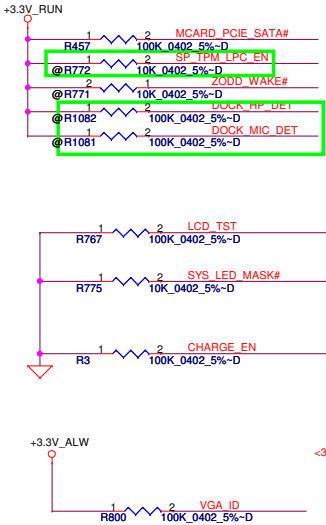
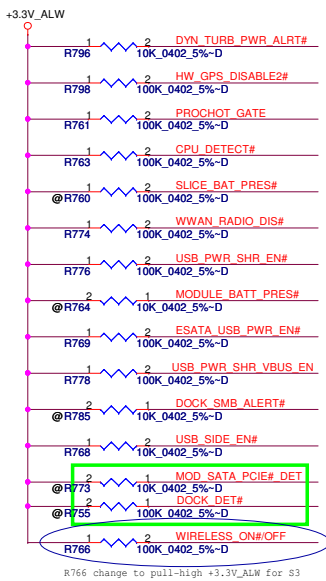


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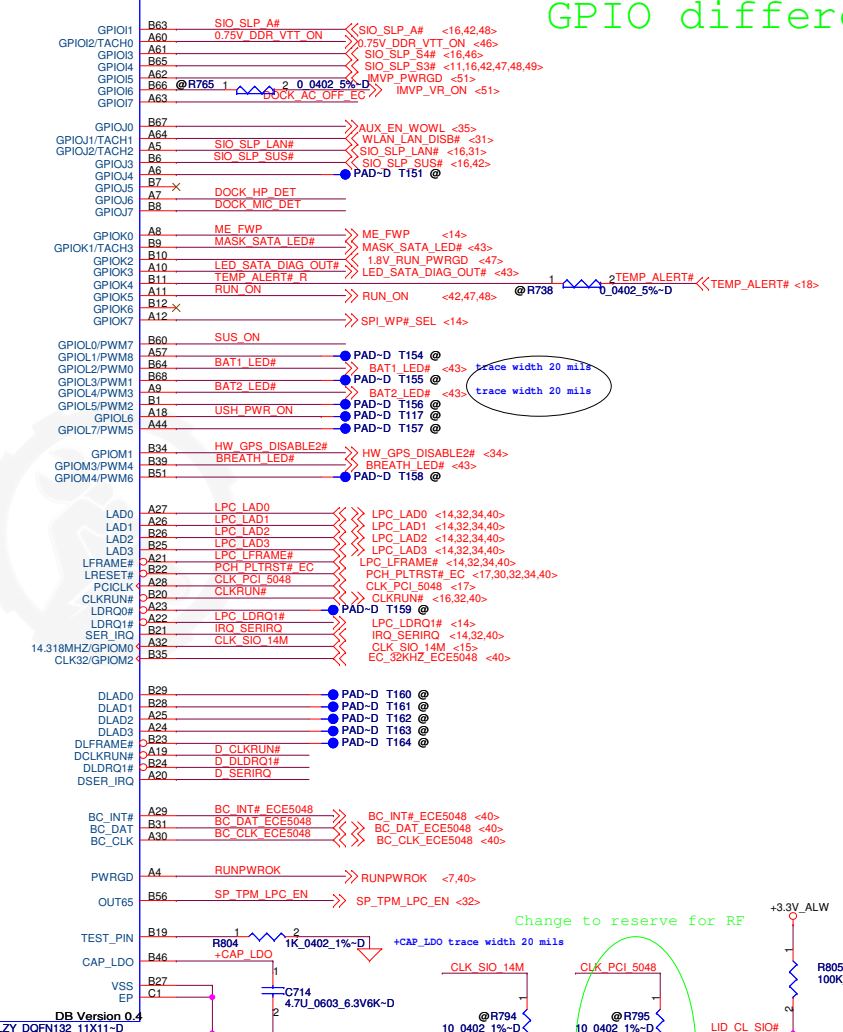
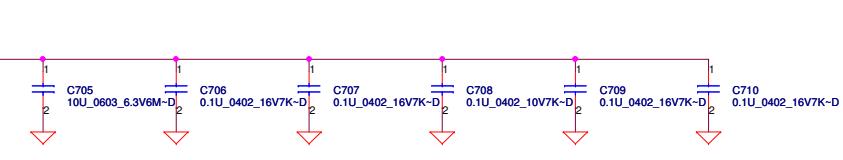
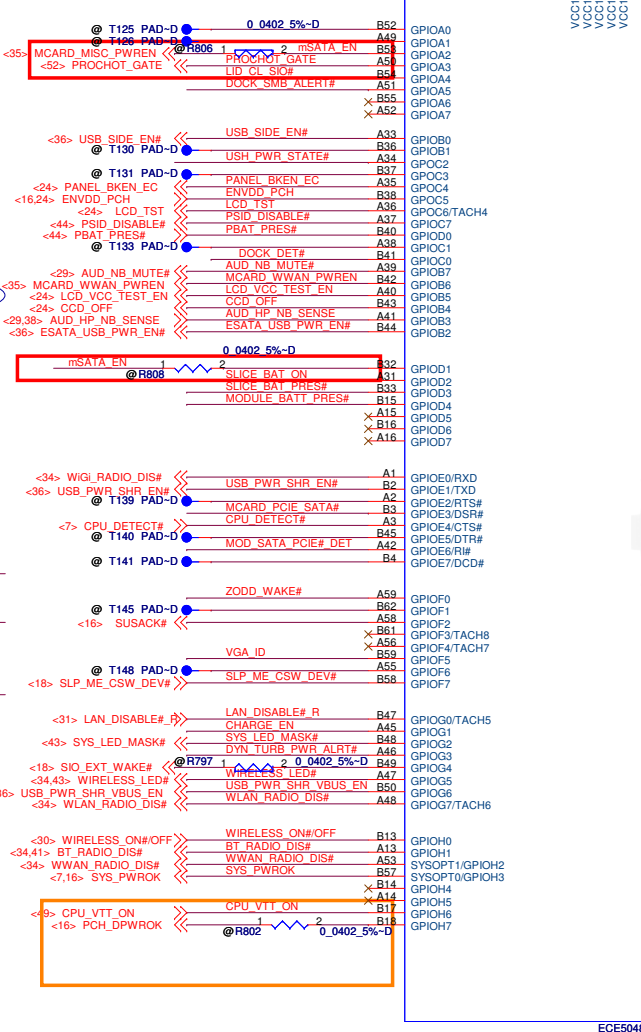
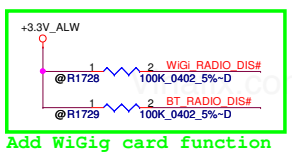
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Title		RJ45
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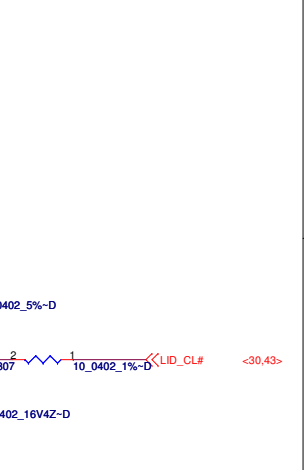
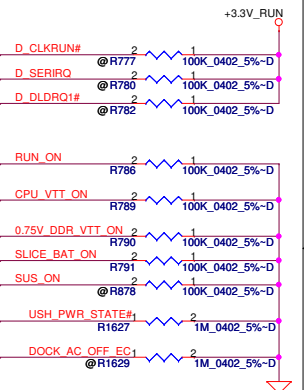
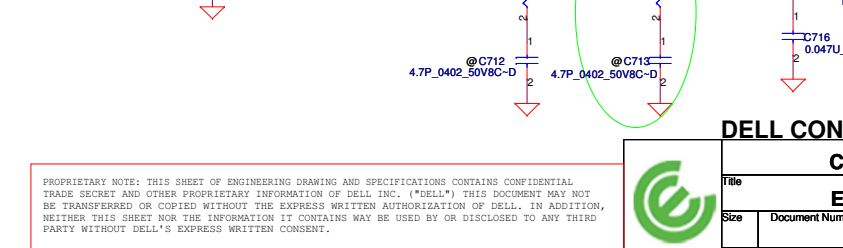
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D12" does not support E-Module, ECE5048(U46) pin B7,A15,B15,A16,B32,A42,A49 not used, but do not assign GPIO for these pins.



GPIO different

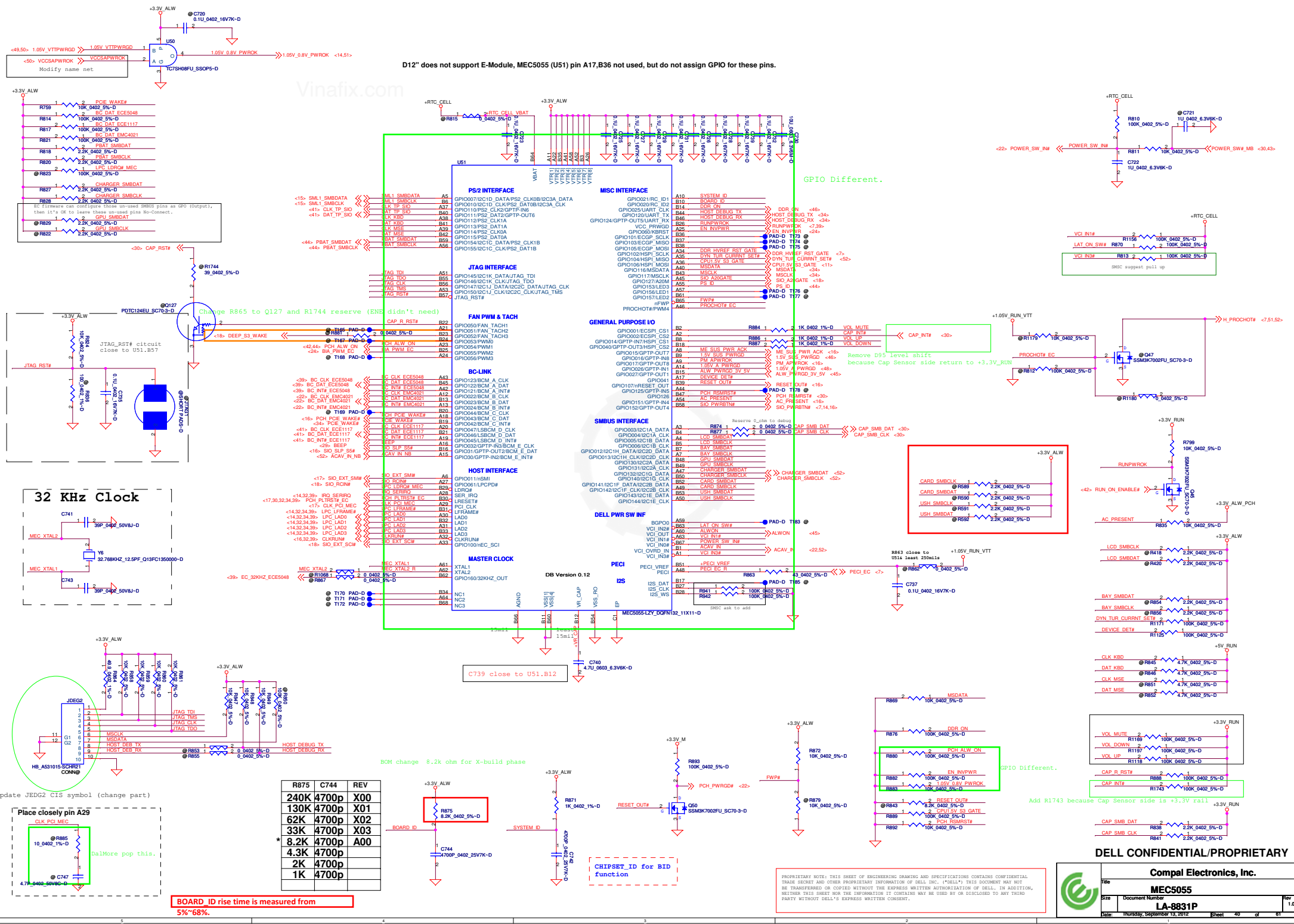


	VGA_ID0
Discrete	0
UMA	1

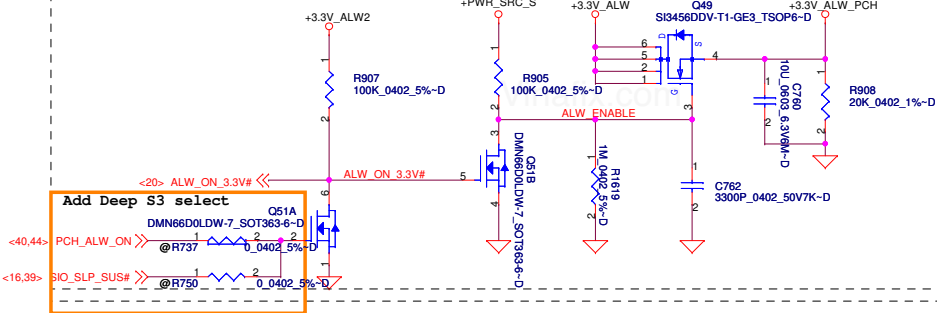
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Cepel Electronics, Inc.		
E5048		
Size	Document Number	Rev
	LA-8831P	1.0
Date	Thursday, September 13, 2012	Sheet 39 of 61

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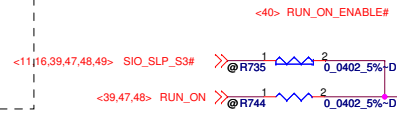


+3.3V_ALW_PCH Source

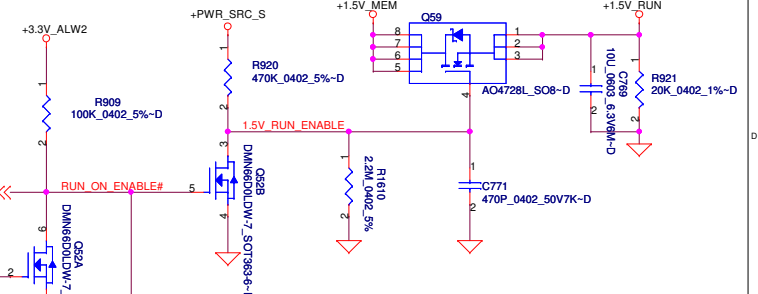


Del +3.3V_SUS for USB power

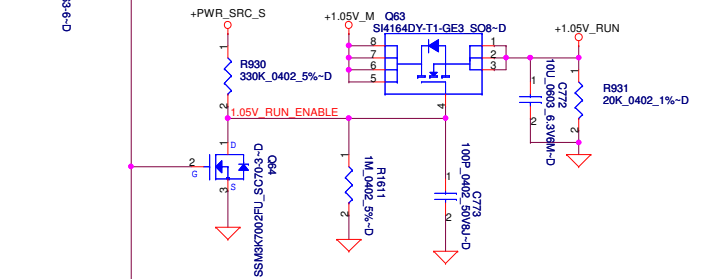
DC/DC Interface



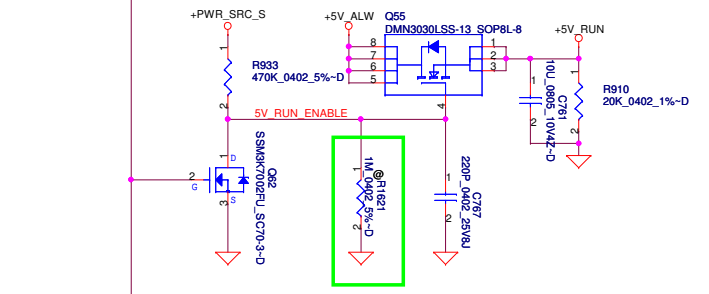
+1.5V_RUN Source



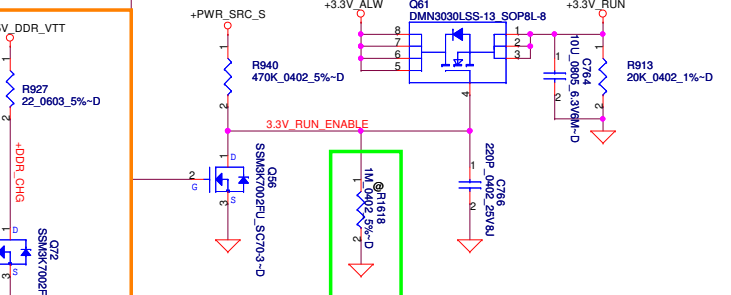
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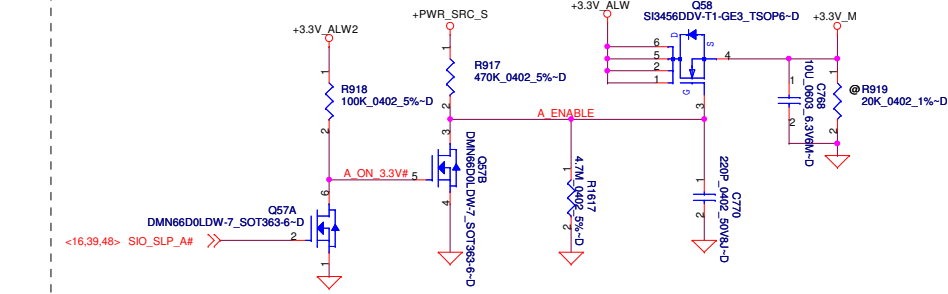
+5V_RUN Source



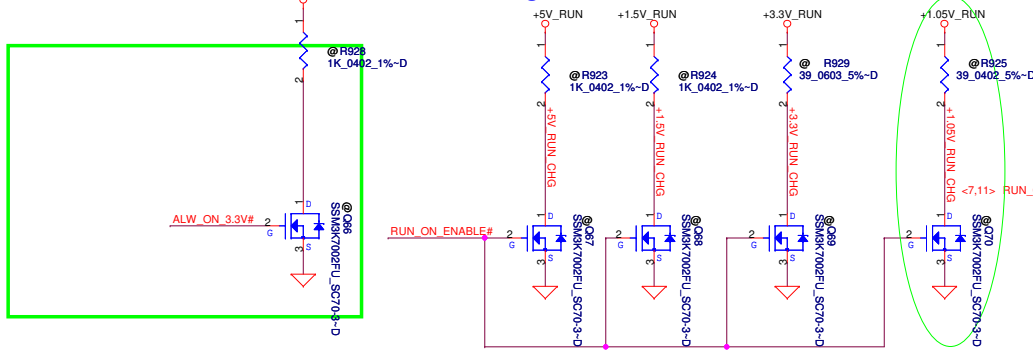
+3.3V_RUN Source



+3.3V_M Source



Discharge Circuit



Change R925 and Q70 to de-pop (reserve)

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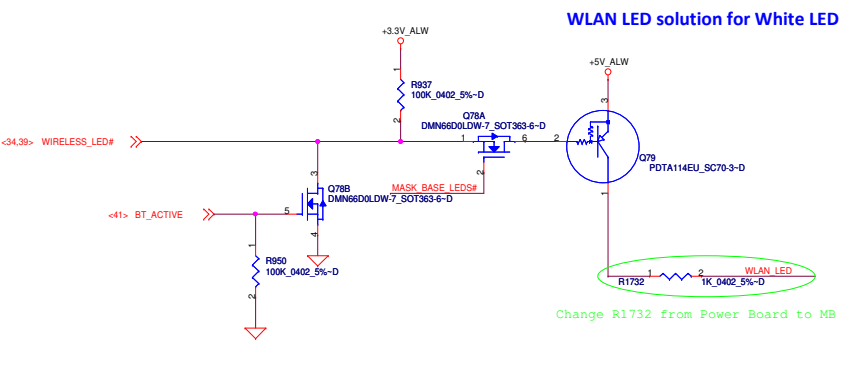
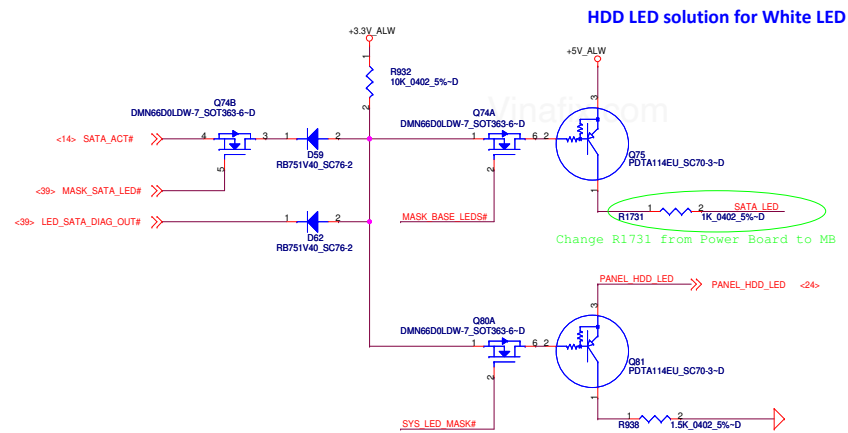
Compal Electronics, Inc.

POWER CONTROL

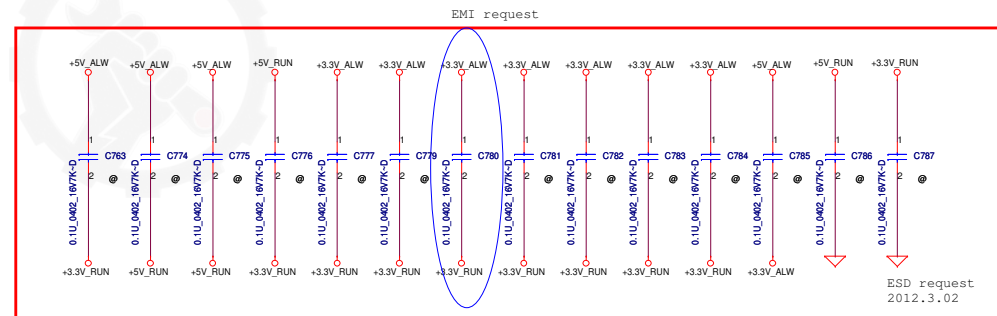
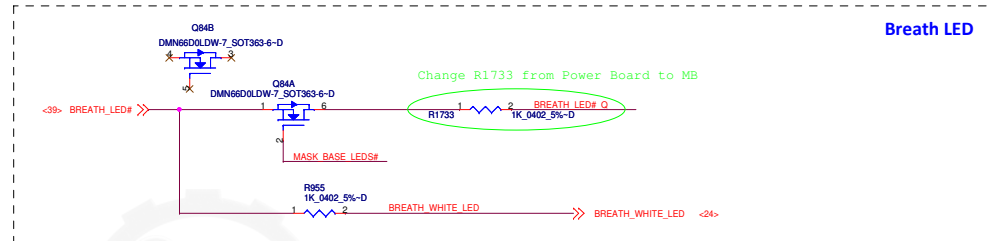
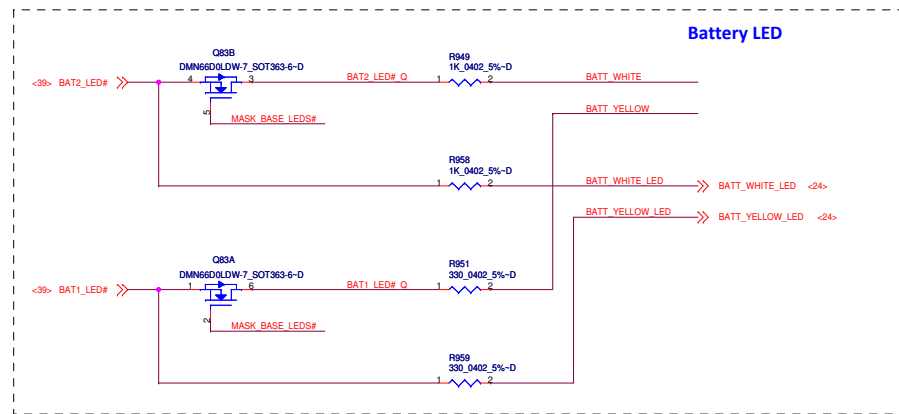
LA-8831P

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Date:	Thursday, September 13, 2012	Sheet 42 of 61

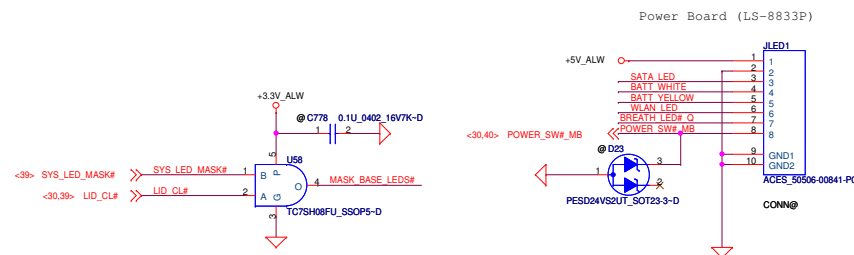
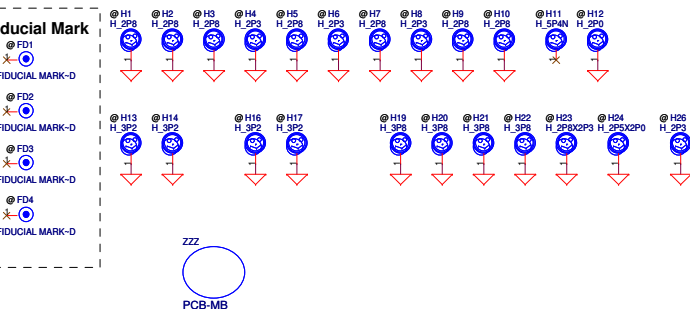
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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



ESD request
2012.3.02



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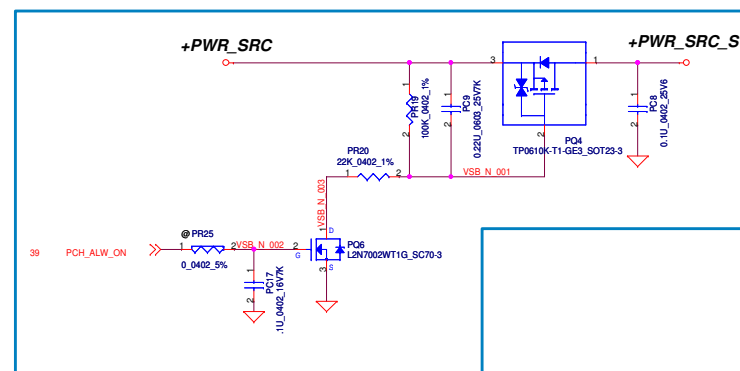
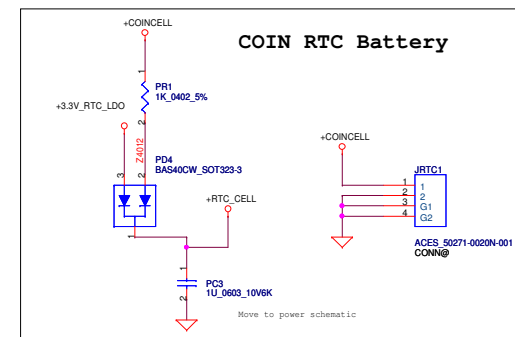
Compal Electronics, Inc.

PAD and Standoff

LA-8831P

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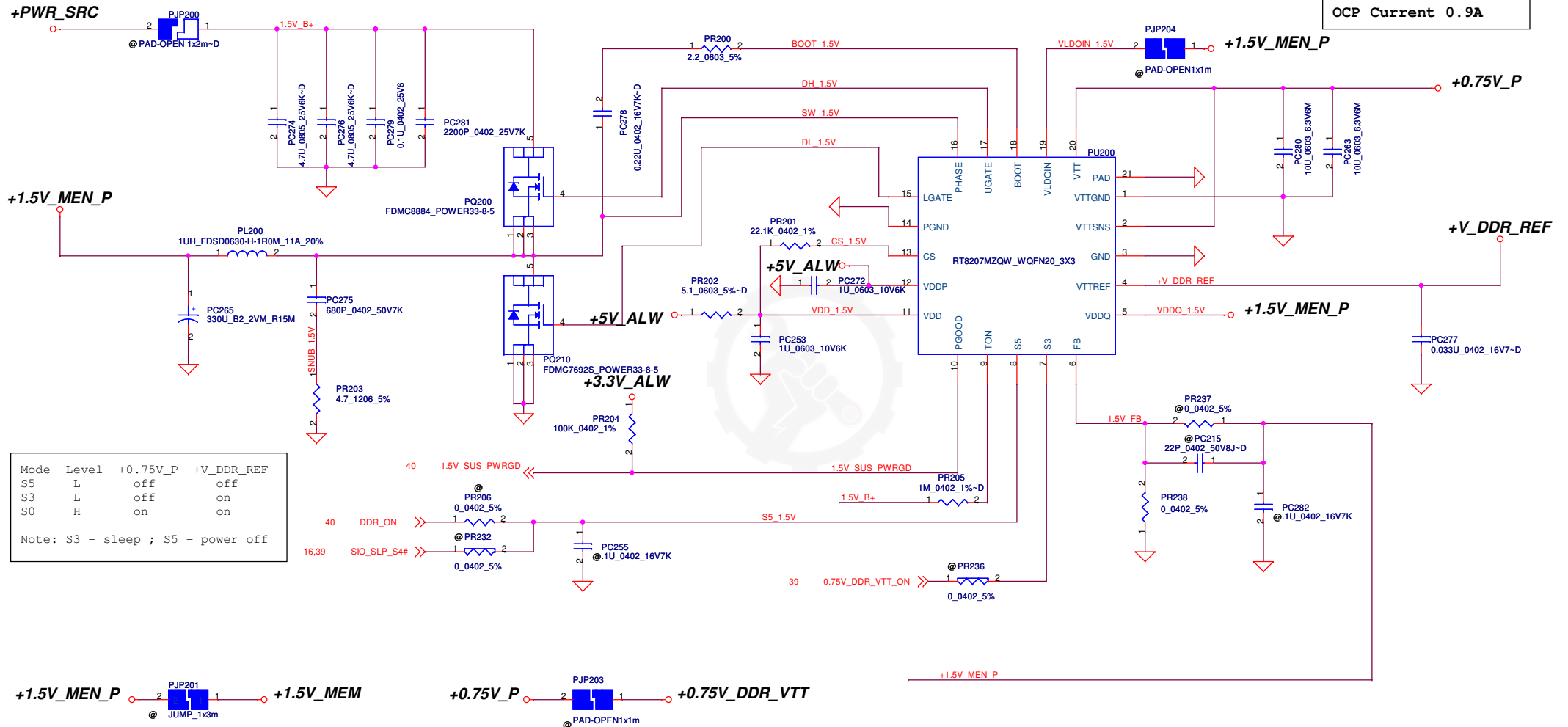
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1.5Volt +/- 5%
TDC 9.11A
Peak Current 13.0A
OCP current 16.9A

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



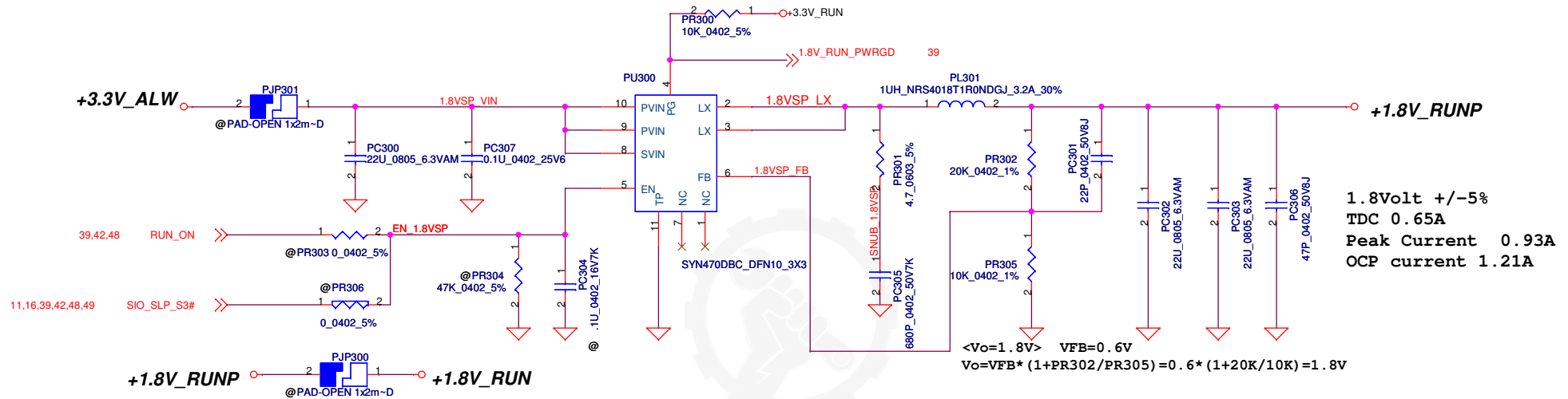
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Title		
+1.5V_MEN/+0.75V_DDR VTT		
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Title

+1.8V_RUN

Size

Document Number

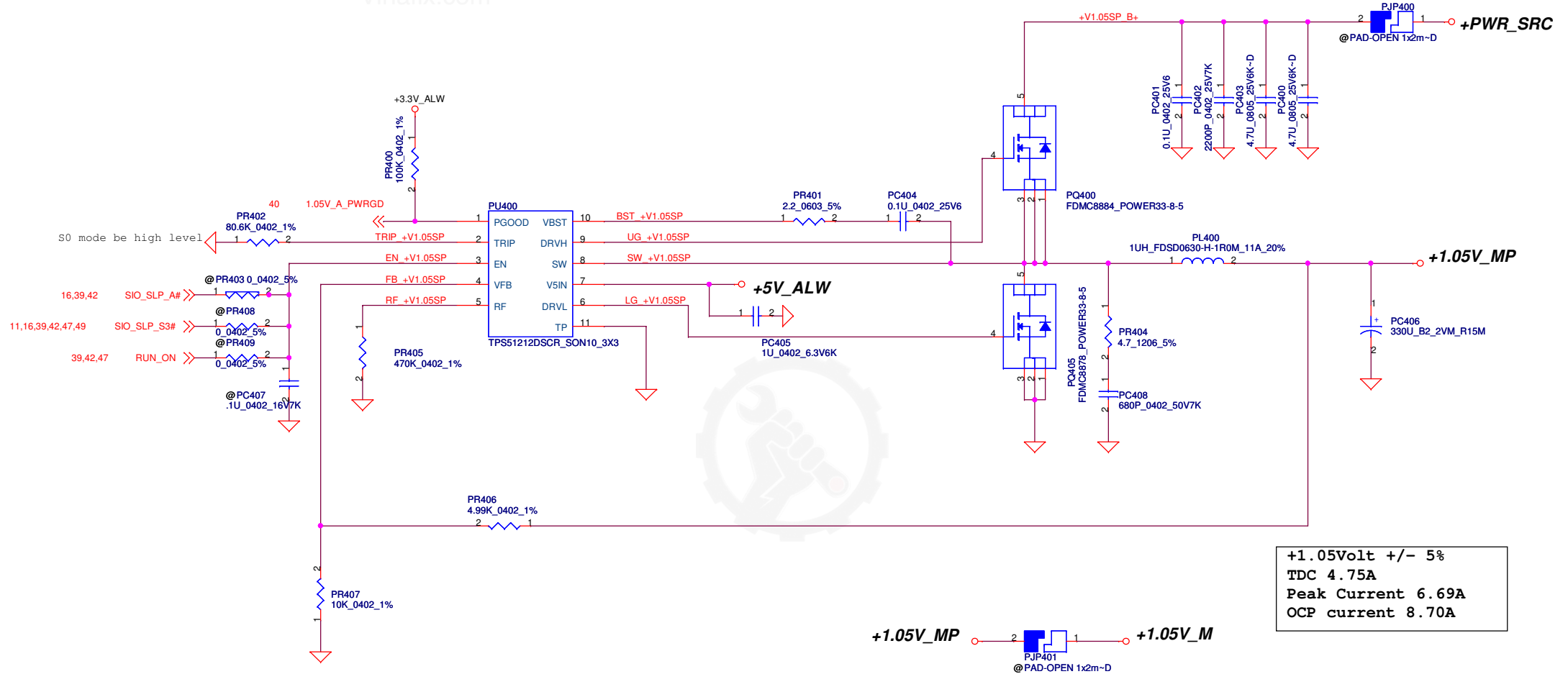
LA-8831P

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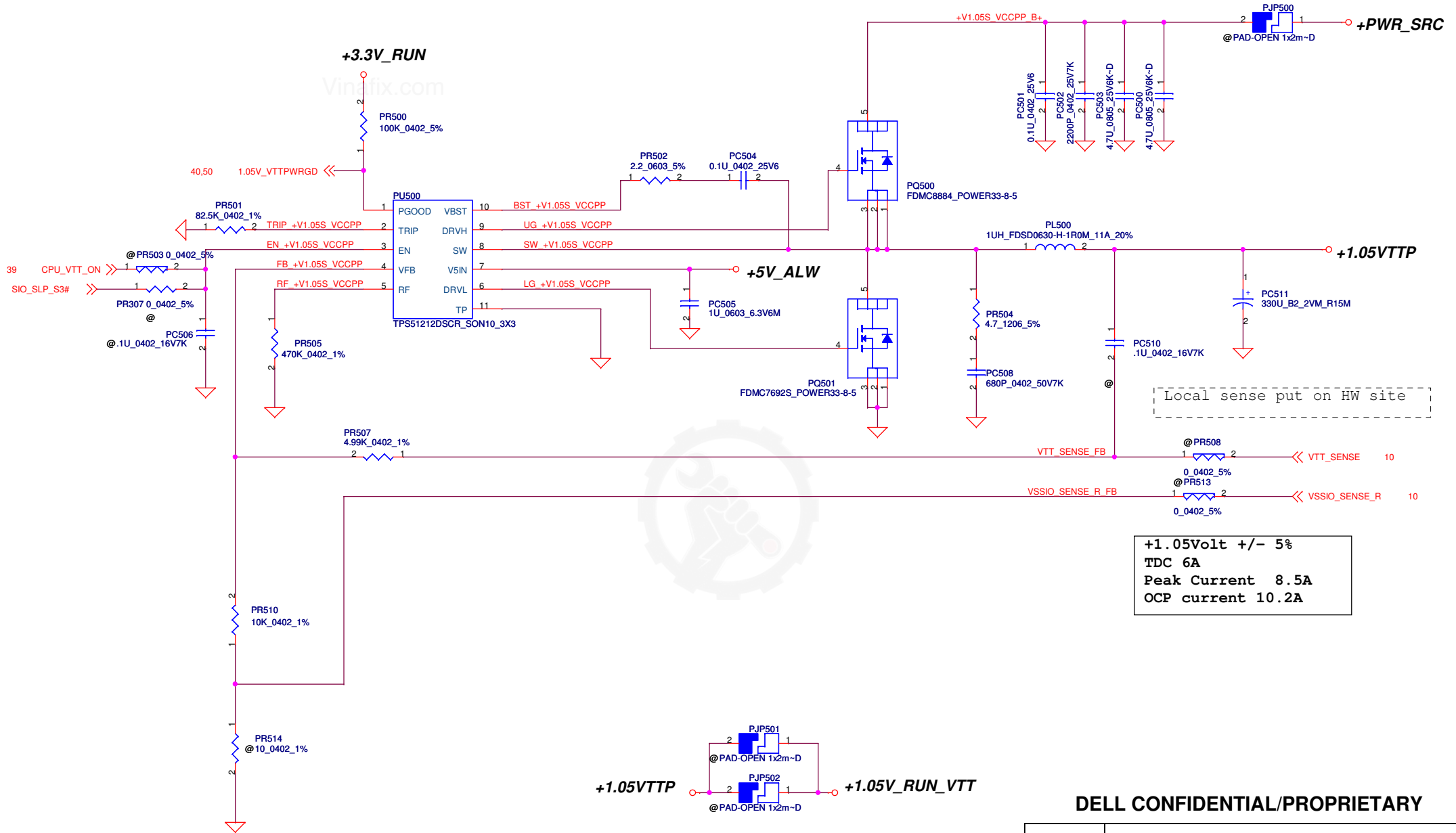
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+1.05V_M			
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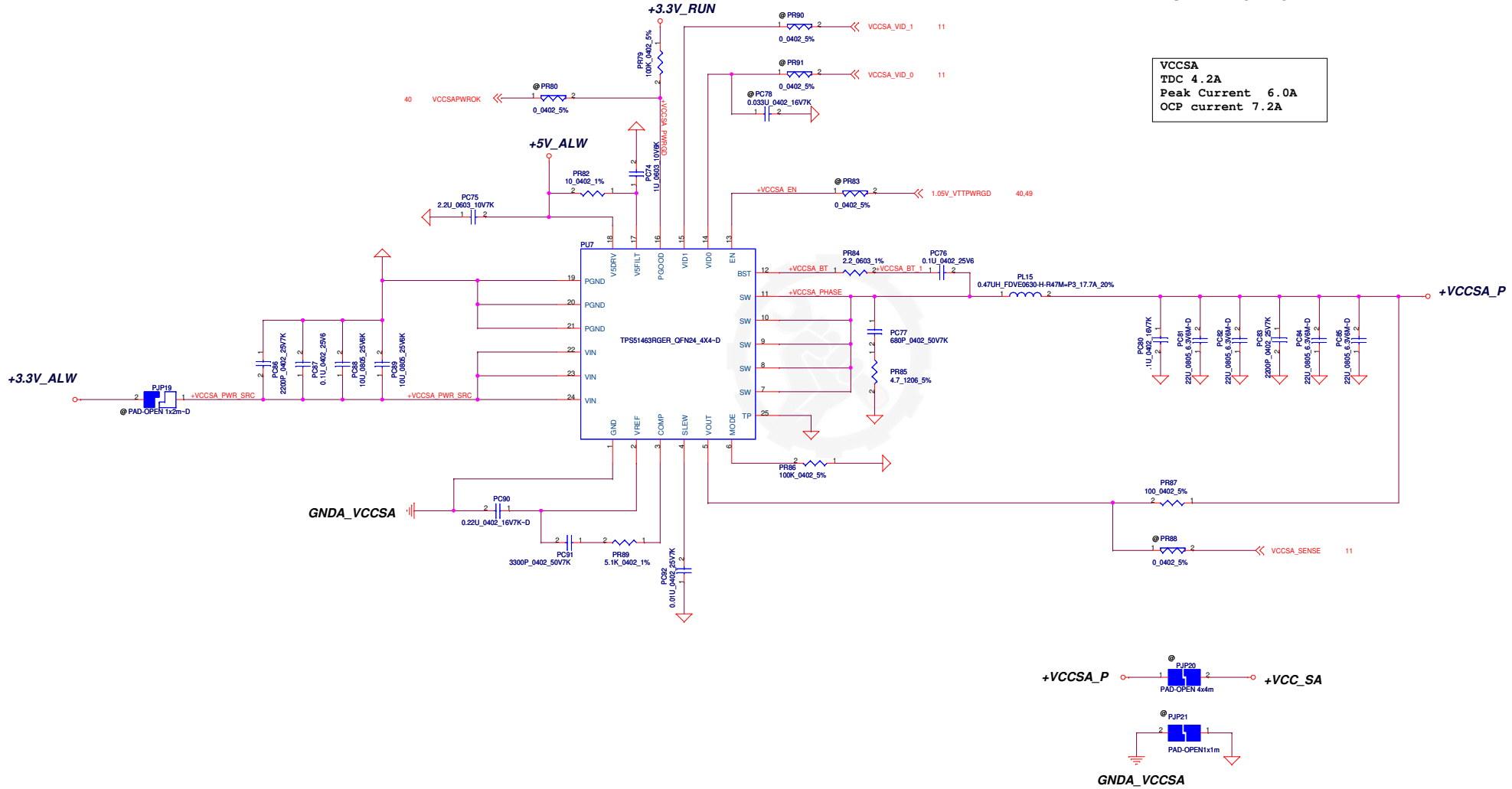
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Compal Electronics, Inc.		
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+1.05V_RUN_VTT		
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The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.750V

output voltage adjustable network

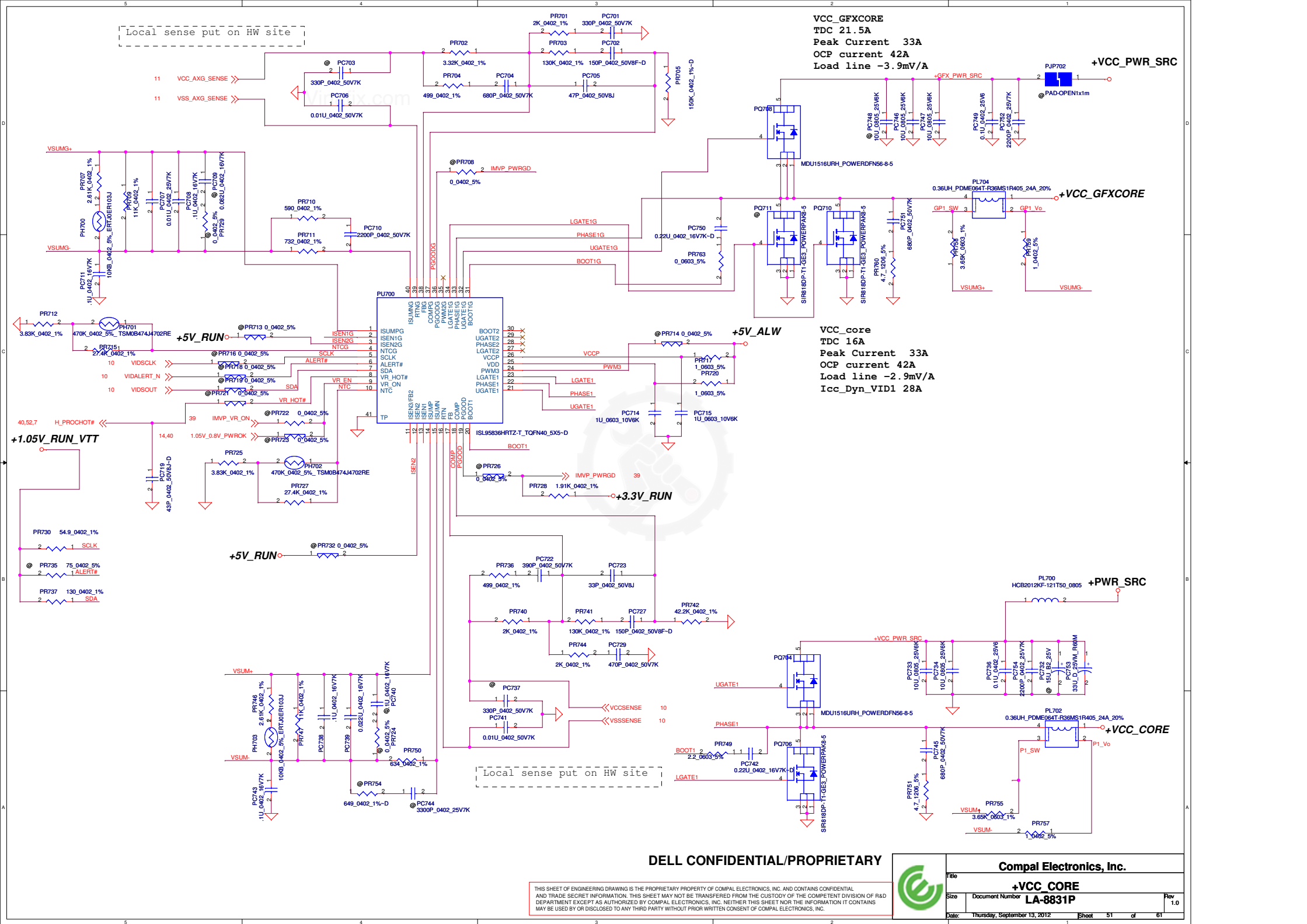
VCCSA
TDC 4.2A
Peak Current 6.0A
OCP current 7.2A



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+VCC SA	
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ISL88731C 11@
BQ24747 22@

E2 AC_OK=17.7 Volt

PR1313
TI bq24745 = 316K
Intersil ISL88731 = 226K

Vref
TI bq24747 = 3.3V
Intersil ISL88731C = 3.2V
VDDP
TI bq24747 = 6V
Intersil ISL88731C = 5.1V

Maximum charging current is 7.2A

DYN_TUR_CURRENT_SET#	
65W	High
90W	Low

Adapter Protection Circuit for Turbo Mode

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Charger

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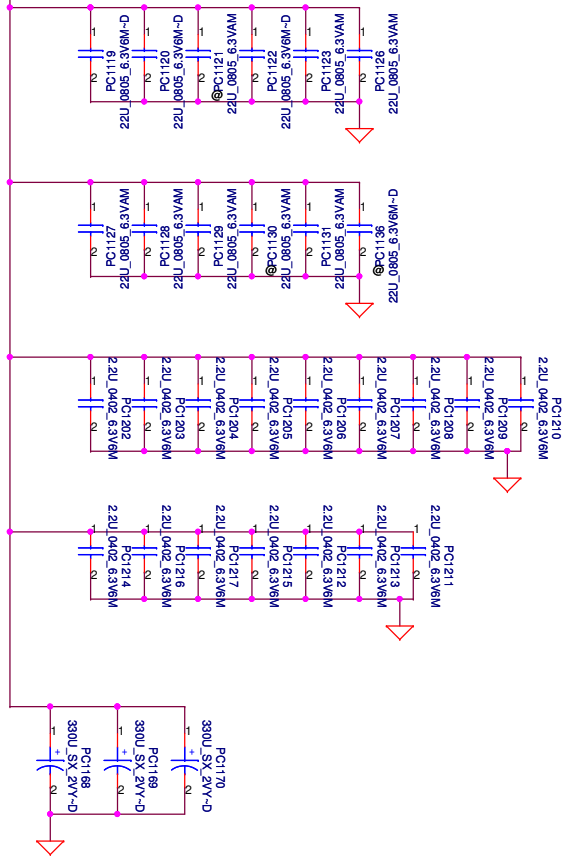
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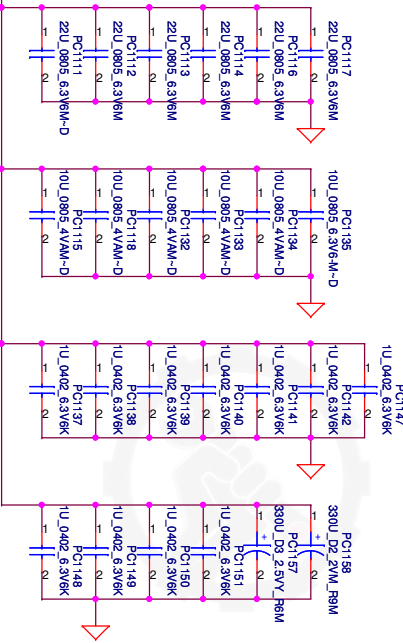


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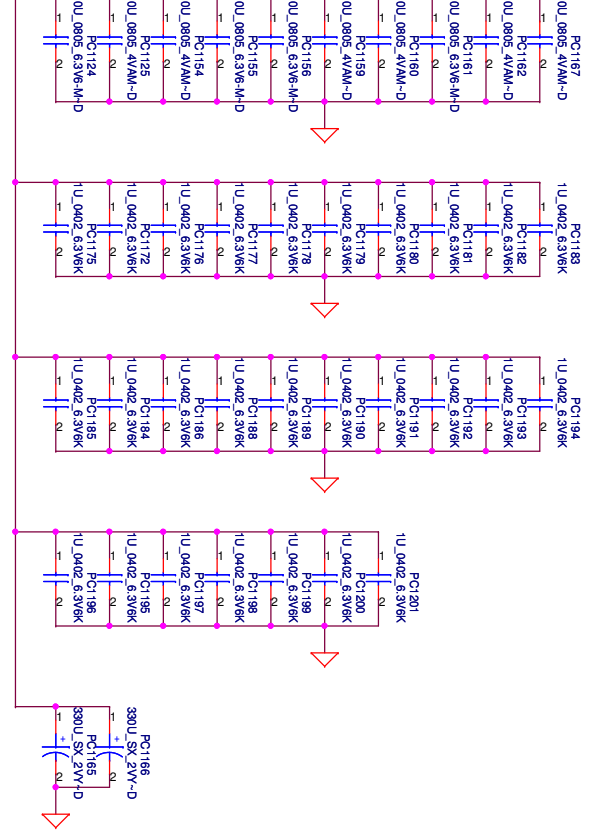
+VCC_CORE



+VCC_GFXCORE



+1.05V_RUN_VTT



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PROCESSOR DECOUPLING		
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Version Change List (P. I. R. List)

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	Power	4/6	Compal	For ESD request	PBATT1 pin6 connect to PQ6.3	X01
2	54	Power	4/6	Compal	For ME design change	Change PC1157 to SGA00004700 Change PC1158 to SGA00004200	X01
3	54	Power	4/11	Compal	For ME design change	Change PC1157 to SGA00006A00	X01
4	54	Power	4/13	Compal	For ME design change	Change PC1158 to SGA00006100	X01
5	47	Power	4/13	Compal	For RF team request	pop PR301, PC305	X01
6	50	Power	4/13	Compal	For RF team request	pop PC77, PR85	X01
7	51	Power	4/18	Compal	Improve CPU transient response	Add PR729, PR724 but unpop	X01
8	51	Power	4/19	Compal	For reduce acoustic noise	Add PC753 Change PL702, PL704 to SH00000NX00	X01
9	44	Power	4/19	Compal	For ESD request	PBATT1 pin6 connect to PQ6.2 PBATT1 pin4 connect to PQ6.3	X01
10	45	Power	4/23	Compal	For Z height limite	Change PC1306 to 0603	X01
11	45	Power	4/25	Compal	For Z height limite	unpop PC735 and PC748	X01
12	51	Power	5/17	Compal	No space, from un-pop to remove	Delete PC735	X02
13	51	Power	6/15	Compal	For Vcore H/L-side MOSFET cross validation	change PQ704, PQ708 to SB00000S800	X02
14	54	Power	7/5	Compal	Change footprint D2 to D3 for height emphasis	change PC1157 footprint to D3 type	X02
15	52	Power	7/5	Compal	Same components but different CPN	Change PR1347 from SD03442228L to SD034422280	X02
16	50	Power	7/5	Compal	Same components but different CPN	Change PC81, PC82, PC84, PC85 CPN from SE000001120 to SE00000111L	X02
17	51	Power	7/12	Compal	For DFB request, PL702 and PL704 pad are too big that will cause components shift	Change PL702, PL704 footprint to CYNTE_PDME064T-R36MS1R405_4P	X02
18	45	Power	8/21	Compal	To meet cpk>1.33 of WCEPTA report	Change PR106 to 90.9 Kohm Change PR105 to 162 Kohm	X03
19	46	Power	8/21	Compal	To meet cpk>1.33 of WCEPTA report	Change PR201 to 22.1 Kohm	X03
20	48	Power	8/21	Compal	To meet cpk>1.33 of WCEPTA report	Change PR402 to 80.6 Kohm	X03
21	49	Power	8/21	Compal	To meet cpk>1.33 of WCEPTA report	Change PR501 to 82.5 Kohm	X03
22	44	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR25	X03

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23	45	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR116, PR100	X03
24	46	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR232, PR236	X03
25	47	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR306	X03
26	48	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR403	X03
27	49	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR513, PR503, PR508	X03
28	50	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR90, PR91, PR80, PR88, PR83	X03
29	51	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR721, PR713, PR726, PR723, PR716, PR714, PR718, PR732, PR719	X03
30	52	Power	8/21	Compal	Reduce 0 ohm resistor	Short PR1342, PR1320, PR1331, PR1339	X03
31	44-54	Power	9/6	Compal	change 80 end PN to 8L, unite with EE	change PC17, PC1316, PC708, PC743, PC738, PC1328, PC255, PC282, PC740, PC711, PC304, PC80, PC407, PC510, PC506 PN from SE076104K80 to SE076104K8L	X03
32	44-54	Power	9/6	Compal	change 80 end PN to 8L, unite with EE	change PC1304, PC1334, PC16, PC8, PC14, PC4, PC736, PC13, PC100, PC1303, PC1305, PC104, PC1310, PC116, PC11, PC1329, PC1302, PC749, PC279, PC1333, PC76, PC307, PC1313, PC404, PC1335, PC401, PC87, PC501, PC504 PC1342 PN from SE00000G880 to SE00000G88L	X03
33	44-54	Power	9/6	Compal	change 80 end PN to 8L, unite with EE	change PC120, PC1336, PC121, PC1338, PC1341, PC1339 PN from SE071101J80 to SE071101J8L	X03
34	44-54	Power	9/6	Compal	change 80 end PN to 8L, unite with EE	change PC263, PC107, PC280 PN from SE000005T80 to SE000005T8L	X03
35	44-54	Power	9/6	Compal	change 80 end PN to 8L, unite with EE	change PC1327, PC3, PC253, PC115, PC117 PC715, PC714, PC272, PC1309, PC74, PC1311 PN from SE080105K80 to SE080105K8L	X03
36	44-54	Power	9/6	Compal	change 80 end PN to 8L, unite with EE	change PC1139, PC1192, PC1201, PC1199, PC1149, PC1176, PC1137, PC1191, PC1188, PC1185, PC1190, PC1148, PC1178, PC1147, PC1184, PC1182, PC1142, PC1189, PC1151, PC1196, PC1183, PC1193, PC1181, PC1198, PC1175, PC1200, PC1186, PC1180, PC1194, PC1150, PC1140, PC405, PC1177, PC1138, PC1197, PC1141, PC1195, PC1172, PC1179 PN from SE000000K80 to SE000000K8L	X03

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Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	HW	04/09/2012	COMPAL	Leakage +3.3V_RUN	R838,R841 Pin 1 change to +3.3V_RUN	X02
2	40, 30	HW	04/09/2012	COMPAL	From ENE reset	JCAP2 Pin5 add R865 to CAP_RST#	X02
3	34	HW	04/09/2012	COMPAL	Leakage +3.3V_RUN	R695 Pin1 change to +3.3V_RUN	X02
4	40	HW	04/09/2012	COMPAL	Leakage +3.3V_RUN	R888 Pin1 change to +3.3V_RUN	X02
5	43	ME	04/10/2012	COMPAL		ADD H25	X02
6	43	ME	04/10/2012	COMPAL		Del H15,H18	X02
7	36	HW	04/10/2012	COMPAL	Follow from E4 solution	Change BOM Q53 Reserve. Change R1614 to 10k ohm	X02
8	36	HW	04/10/2012	COMPAL	Follow from E4 solution	Change U2 SA00004RE0L to SA00004VH00	X02
9	36	HW	04/11/2012	COMPAL	HDMI power solution	Del D4, R1648 and F2, Add U76 AP2330W-7	X02
10	36	HW	04/11/2012	COMPAL	Cost saving	Change U48 to SA00003TV00,Del R748	X02
11	43	HW	04/11/2012	COMPAL	Follow from E4 solution	Change PANEL_HDD_LED to Q81 Pin 3, ADD R938 (1.2k) to Q83 Pin1	X02
12	18	HW	04/11/2012	COMPAL	Follow from E4 solution	Del RH366	X02
13	6, 9	HW	04/12/2012	COMPAL	Follow from E4 solution	Del RC20,RC21 Change to T110,T128	X02
14	34	HW	04/12/2012	COMPAL		Change BOM C1176, C609 Reserve	X02
15	34, 39	HW	04/12/2012	COMPAL		Add R753 Connect "BT_WIGIG_RADIO_DIS#" to JMINI2 Pin51	X02
16	34, 39	HW	04/12/2012	COMPAL		Add R739 Connect "WIGIG_RADIO_DIS#" to JMINI2 Pin39	X02
17	34	18	04/12/2012	COMPAL		Change BOM C1310,C1309,C617,C618 to 0.01UF	X02
18	34	HW	04/12/2012	COMPAL	Reserve for RF	Delete C1176, Change C609 to Reserve	X02
19	34, 39	HW	04/12/2012	COMPAL	Add WiGig card function 1/3	Add trace that 5048.A1 to JMINI2.32 of WiGi_RADIO_DIS# 5048.A13 to JMINI2.51 of BT_RADIO_DIS#	X02
20	34, 39	HW	04/12/2012	COMPAL	Add WiGig card function 2/3	Reserve path selection R1726, D92 and R1727, D93 Reserve +3.3V_ALW pull-high resistor R1728, R1729	X02
21	41	HW	04/12/2012	COMPAL	Add WiGig card function 3/3	Add R1730 and reserve D94 to prevent leakage for BT_RADIO_DIS# to BTRADIO_DIS#_CON	X02

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EE P.I.R (1/4)

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	40	HW	04/12/2012	COMPAL	Board ID change	Change R875 to 62K	X02
23	38	HW	04/12/2012	COMPAL	Improve LAN layout	Swap TR1(X'FORM) LAN signals (From 0,1,2,3 to 3,2,1,0). Swap C36~C39	X02
24	29	HW	04/13/2012	COMPAL	EMI fail on Audio_SPK	Add C1318~C1321 (0402 330pF SE074331K8L)	X02
25	19, 43	HW	04/13/2012	COMPAL	EMI request	Pop C1247, C780	X02
26	11	HW	04/13/2012	COMPAL	Improve power consumption	Change RC72 to 330k ohm, RC143 to 1M ohm and CC136 to 0.022UF	X02
27	18	HW	04/13/2012	COMPAL	BOM control for TPM and DTP	RH267 -> TPM@, RH270 -> DTP@	X02
28	32	HW	04/13/2012	COMPAL	BOM control for TPM	R659 and R660 change to TPM@	X02
29	32	HW	04/13/2012	COMPAL	PCI CLK EA fail	de-pop RE5 and RE3 (@ only)	X02
30	19	HW	04/16/2012	COMPAL	TAIYO didn't support 0603 size	LH8 change Vendor to SHI00004Q0L (TDK)	X02
31	25	HW	04/16/2012	COMPAL	HDMI EMI request	Change R451,R459,R462,R466,R468~R471 to L116~L123 (9nH, SHI0000EE0L) and pop, de-pop L19~L22	X02
32	24	HW	04/16/2012	COMPAL	Saving more spacing for DFB concern	Remove D38	X02
33	37	HW	04/17/2012	COMPAL	Add BOM config for w/ and w/o eSATA redriver	7@ for w/ eSATA redriver, 8@ for w/o eSATA redriver	X02
34	20	HW	04/17/2012	COMPAL	Add current limitation (PCH)	Change RH215 from 0_0402 to 0_0603	X02
35	15	HW	04/17/2012	COMPAL	Reserve unuse signal (FLEX CLK)	Reserve RH315, changing to de-pop	X02
36	42	HW	04/17/2012	COMPAL	Reserve charge circuit	Change R925 and Q70 to de-pop (Reserve)	X02
37	34	HW	04/17/2012	COMPAL	Reserve RF circuit for SIM card	Change C628~C631 to de-pop (Reserve)	X02
38	36, 37	HW	04/17/2012	COMPAL	ESD request ESD Diode for USB3.0	D78, D88, D89 change to NXP SC30000250L	X02
39	17	HW	04/17/2012	COMPAL	RF request for PCI CLK	Add CH111 10p for CLK_PCI_LOOPBACK and CH112 10p for CLK_PCI_TPM_TCM	X02
40	19	HW	04/17/2012	COMPAL	RF request	Add C1322 and pop C1248 for +3.3V_ALW and +5V_ALW	X02
41	38	HW	04/17/2012	COMPAL	EMI request reserve for LAN LED signal	Reserve C1323~C1325 120p cap	X02
42	40	HW	04/18/2012	COMPAL	Cap sensor didn't need reset signal (IC internal reset)	Change R865 to reserve	X02
43	39	HW	04/18/2012	COMPAL	CLK_PCI_5048 EA fail	Change R795 and C713 to reserve	X02
44	17	HW	04/18/2012	COMPAL	RF request for CLK_PCI_MEC and CLK_PCI_5048	Pop CH109 and CH110 with 10pF cap	X02
45	24	HW	04/18/2012	COMPAL	Layout request	Swap D9 pin2 and pin3 (DMIC0 and DMIC_CLK)	X02
46	31, 38	HW	04/18/2012	COMPAL	EMI request for LAN signal	Add L124~L131 with 12nH for LAN signals	X02

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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
47	43	HW	04/18/2012	COMPAL	LED design change	Change R1731, R1732, R1733 with 1.2k ohm from Power Board (LS-8833P) to MB	X02
48	41	HW	04/19/2012	COMPAL	Design change	Change L54 and L55 to 0402 size (SM01000C500)	X02
49	24, 29	HW	04/19/2012	COMPAL	Design change	Change LE3 and LE92 to 0402 size (SM01000BV0L)	X02
50	14, 34, 37, 41	HW	04/19/2012	COMPAL	Connector Symbol update	Update JTP1, JTAA1, JSIM1, JESA1, JDEG2	X02
51	24	HW	04/19/2012	COMPAL	LVDS PWM and BKEN control by PCH only	Change D68 and D69 to reserve	X02
52	34	HW	04/19/2012	COMPAL	WWAN card didn't have PCIE bus for this project	Change R725 to reserve	X02
53	39	HW	04/19/2012	COMPAL	WIRELESS_ON#/OFF on S3 need pull-high to ALW power	Change R766 to pull-high +3.3V_ALW	X02
54	37	HW	04/19/2012	COMPAL	eSATA re-driver need to meet 2nd source design	Change to pop R766	X02
55	19, 20, 31	HW	04/20/2012	COMPAL	Replace by other Vendor	Change LH6, LH7, LH8, L29	X02
56	11, 12, 13	HW	04/23/2012	COMPAL	ME H-limitation	Change CC167, CD16 and CD38 to SGA00006A00 H=1.4mm	X02
57	29	HW	04/23/2012	COMPAL	ME H-limitation	Change C954, C955, C958, C960, C966 to SE00000SU00 (0603 10U cap)	X02
58	23	HW	04/23/2012	COMPAL	Cost saving	Change L102, L103 to 0402 size, L99~L101 to 0402 SM01000FH0L	X02
59	43	HW	04/25/2012	COMPAL	ME change screw size	Change H13, H14, H16 H17 from 3.3 to 3.2	X02
60	43	HW	04/25/2012	COMPAL	ESD pop small board protection circuit	Change D23 to reserve	X02
61	40	HW	06/26/2012	COMPAL	Cap Sensor Power rail change to only +5V_RUN	Change R838 and R841 to pull-high to +5V_RUN	X03
62	34	HW	06/26/2012	COMPAL	WiGi Card support BT_LED control	Add BT_LED# (JMINI2.46) with Q126 and R1734	X03
63	29	HW	06/26/2012	COMPAL	Improve Internal Speaker R/L cable swap	Swap JSPK1 pin-define	X03
64	31	HW	06/26/2012	COMPAL	Improve IEEE LAN EA	Add R1735~R1742 (6.8ohm) and C1326~C1329 (3.3p) for IEEE LAN EA	X03
65	30	HW	06/26/2012	COMPAL	Cap Sensor Power rail change to only +5V_RUN	Change JCAP.2 to +5V_RUN	X03
66	24	HW	06/26/2012	COMPAL	For LCD test Mode	Pop D68, D69	X03
67	40	HW	06/26/2012	COMPAL	Crystal test result	Change C741 and C743 to 39p cap (SE071390J8L)	X03
68	24	HW	06/26/2012	COMPAL	ME limitation	Change C300 to 10p 0603 size (SE00000SU00)	X03
69	36	HW	06/26/2012	COMPAL	USB2.0 port0 EA	Change L51 to SM070001600	X03
70	34	HW	06/26/2012	COMPAL	Support WiGi Card	Pop D92, D93	X03
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Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
71	23	HW	06/26/2012	COMPAL	New solution for CRT power	Change D80, F3 and R1640 to U77 (SA00004ZA00)	X03
72	40	HW	06/28/2012	COMPAL	Cap Sensor change power rail to +5V_RUN	Replace R868 by D95 (SC100000S0L) and add R1743 for CAP_INT#_R	X03
73	30	HW	06/28/2012	COMPAL	ME change JSC1 and JLID1 position from BOT to TOP	Swap JSC1 and JLID1 pin-define	X03
74	30	ME	06/28/2012	COMPAL	ME add Screw	Add H26 H_2P3	X03
75	43	ME	07/02/2012	COMPAL	ME testing result	ME Change H11 to 5P4N	X03
76	30	ME	07/03/2012	COMPAL	Change JLID1 connector	Change JLID1 connector to HB_A080415-SAHR21	X03
77	30	EE	07/03/2012	COMPAL	Change JCAP2 power rail to +5V_RUN	Change C1316 to +5V_RUN	X03
78	40	EE	07/04/2012	COMPAL	Board ID change	Change R875 to 33K	X03
79	43	EE	07/04/2012	COMPAL	LED light testing	Change R1733(1.5K), R1731(600), R949(600), R1732(700) R955(2.2K), R938(2.4K), R958(1.8K)	X03
80	22	EE	07/04/2012	COMPAL	Thermal team design change	Change R406 from 1.24k to 1.82k (92degree to 98degree)	X03
81	11, 12, 13	EE	07/05/2012	COMPAL	Correct SGA00006A00 footprint to D3 size	CD167, CD16, CD38 package size change to D3 H=1.4mm	X03
82	24	EE	07/05/2012	COMPAL	Add RF solution for LVDS	Add C1330 and C1331 to 2200p, C1332 and C1333 to 10p	X03
83	23, 24	EE	07/06/2012	COMPAL	ESD team request	Pop D9 (SCA00000T0L), De-pop D77 and D83	X03
84	24	EE	07/06/2012	COMPAL	Change JLVDS2(Golden Type) and JSC1 connectr	JLVDS2 -> E-T_3703K-F12N-03R(SP02000TJ00), JSC1 -> HB_A081015-SAHR21	X03
85	43	ME	07/09/2012	COMPAL	ME testing result	ME Change H3 to 2P8, keeping H11 to 2P8 (Change to 5P4N next phase)	X03
86	41	EE	07/09/2012	COMPAL	WiGi Card support and use the same BT_RADIO_DIS#	De-pop R1730 and pop D94 (SC100000S0L)	X03
87	40	EE	07/10/2012	COMPAL	Cap Sensor Board change to +5V_RUN power rail	Change reserve from R865 to Q127 and R1744	X03
88	35	EE	07/11/2012	COMPAL	For WWAN power soft-start	Change C644 from 220p to 2200p(SE074222K8L)	X03
89	39, 40	EE	07/11/2012	COMPAL	Change resistors of useless EC GPIO to reserve	De-pop R785, R760, R764, R774, R771, R1082, R1081, R777, R782, R780, R878, R1629 R845, R846, R851, R852, R829, R822, R854, R856, R420, R418	X03
90	7	EE	08/20/2012	COMPAL	Change XDP(IITP) components to reserve	De-pop RC5, RC7, RC8, CC65	A00
91	14	EE	08/20/2012	COMPAL	X76 BOM control for ROM part	Change U52 and U53 to X76@ BOM config	A00
92	14	EE	08/20/2012	COMPAL	Change JTAG resistors on PCH to reserve	De-pop RH47, RH48, RH49 and RH288	A00
93	40	EE	08/20/2012	COMPAL	Change Board ID for X-build (A00)	Change R875 to 8.2k ohm	A00
94	34	EE	08/21/2012	COMPAL	Change +1.5V_RUN cap of Mini Card to reserve because Mini Card didn't have +1.5V_RUN power	De-pop C593, C594, C601, C602, C619, C620	A00
95	43	EE	08/30/2012	COMPAL	LED design change	Change R1731, R1732, R1733, R949, R955, R958 to 1k ohm and R938 to 1.5k ohm	A00
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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
96	31	HW	08/30/2012	COMPAL	IEEE LAN solution modify	Change C1326 from 3.3p to 15p 0402 cap	A00
97	38	HW	08/30/2012	COMPAL	EMI request	Change C1104 from 1000p to 150p 1808 cap (SE00000FA80)	A00
98	43	ME	09/03/2012	COMPAL	Modify ME drawing	Change H11 from H_2P8 to H_5P4N	A00
99	43	HW	09/03/2012	COMPAL	Meet ESD 2nd source request	Change D81, D82 from SCA00000T0L to SCA00001A00	A00
100	30	HW	09/04/2012	COMPAL	Change to +3.3V_RUN for ENE IC	JCAP2.2 and C1316.1 change to +3.3V_RUN	A00
101	40	HW	09/04/2012	COMPAL	Cap Sensor (ENE IC) return to +3.3V_RUN	Remove D95 (EC and ENE both 3.3V power rail)	A00
102	39	HW	09/05/2012	COMPAL	Fei Dao didn't support Dock	De-pop R755 Dock detect resistor	A00
103	7, 17, 30, 31, 40, 41, 43	HW	09/06/2012	COMPAL	Cost reduction plan	De-pop CC156, CC140, CH102, C288, C478, C720 C765, C778, C1278, C1279, C1304	A00
104	40	HW	09/12/2012	COMPAL	ENE IC change to +3.3V_RUN power rail	Change Cap_SMBus R838 and R841 to +3.3V_RUN	A00
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